OLED SPECIFICATION
7.0 Inch 1080*1920 Dots

MODULE NO.: A070081N-V01

Rev：01

Date：2025-04-10

APPROVED	CHECKED	PREPARED

Customer Approval:	☐ Accept ☐ Reject Comment: Approved by:____

History of Version

Date	Ver	Description	PREPARED	Checked
2025-04-10	01	New sample	Zgh	

Table of Contents

1 Module basic Specification

1.1 Module application

- The AMOLED (Active Matrix/Organic Light Emitting Diode) module is composed of 6.97” OLED panel with touch panel, driver circuits, FPC and TP FPC unit.
- This module is display terminals for Handheld game console.
- This module follows RoHS /Reach List of hazardous substances.

1.2 Display Module Specification

1.2.1 Display Panel specification

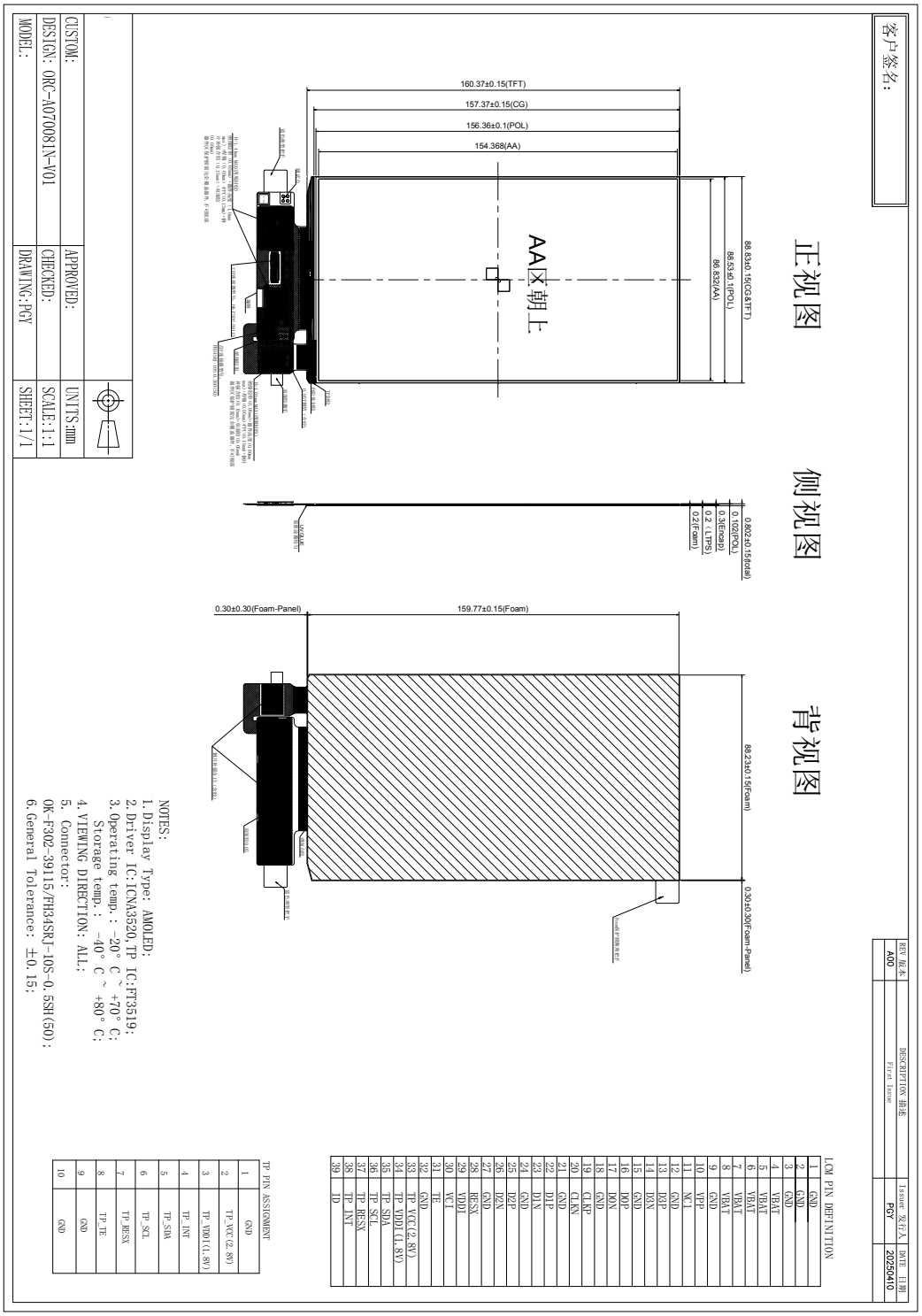
No	Item	Specification	Unit	Remarks
1	Display type	Rigid AMOLED		
2	Display Size	6.97”	Inch	
3	Active Area	Φ86.832*154.368	mm	
4	Pixel Size	0.0804	mm	
5	Pixel Pitch	0.0804	mm	
6	Pixel Per inch	316	PPI	
7	Resolution	1920*1080 SPR		
8	Color Depth	16.7M(24bit)		
9	Frame rate	120HZ		
10	Driver IC (Type)	ICNA3520		
11	Driver IC RAM Size	1/3RAM		
12	Panel bonding type	COG		
13	Interface	MIPI 4Lane		
14	TFT Technology Type	LTPS		
15	Encap glass height	0.3	mm	
16	TFT glass height	0.2	mm	
17	Display Panel size	160.368*88.832*0.5t	mm	
18	Module Size	160.368*88.832*0.802t	mm	
19	Operation Temperature	-20~+70	deg	
20	Storage Temperature	-40~+80	deg	

1.2.2 TP specification

No	Item	Specification	Unit	Remarks
1	TP type	on cell		
2	Channel number	19*35		
3	Pitch	4.5798mm ×4.4158mm	mm	
4	TP interface	I2C		
5	TP IC (Type)&Package	FT3519		

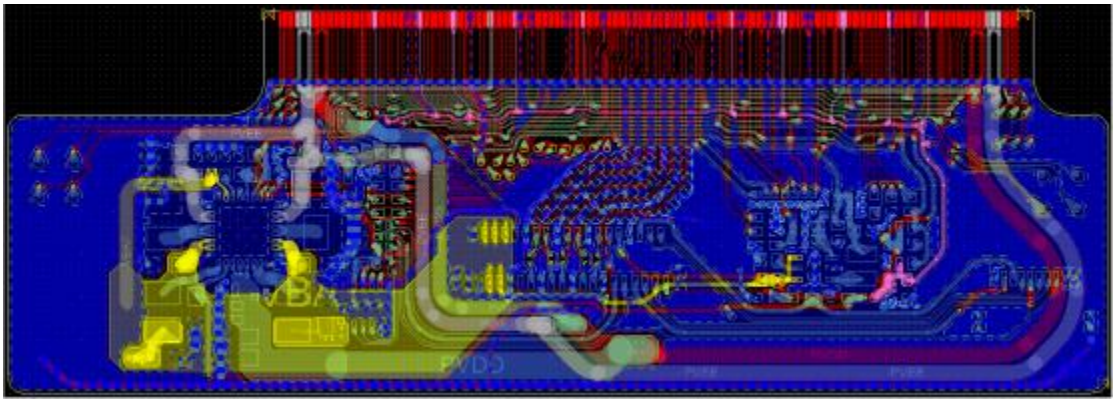
2 Mechanical Drawing

2.1 Module Drawing

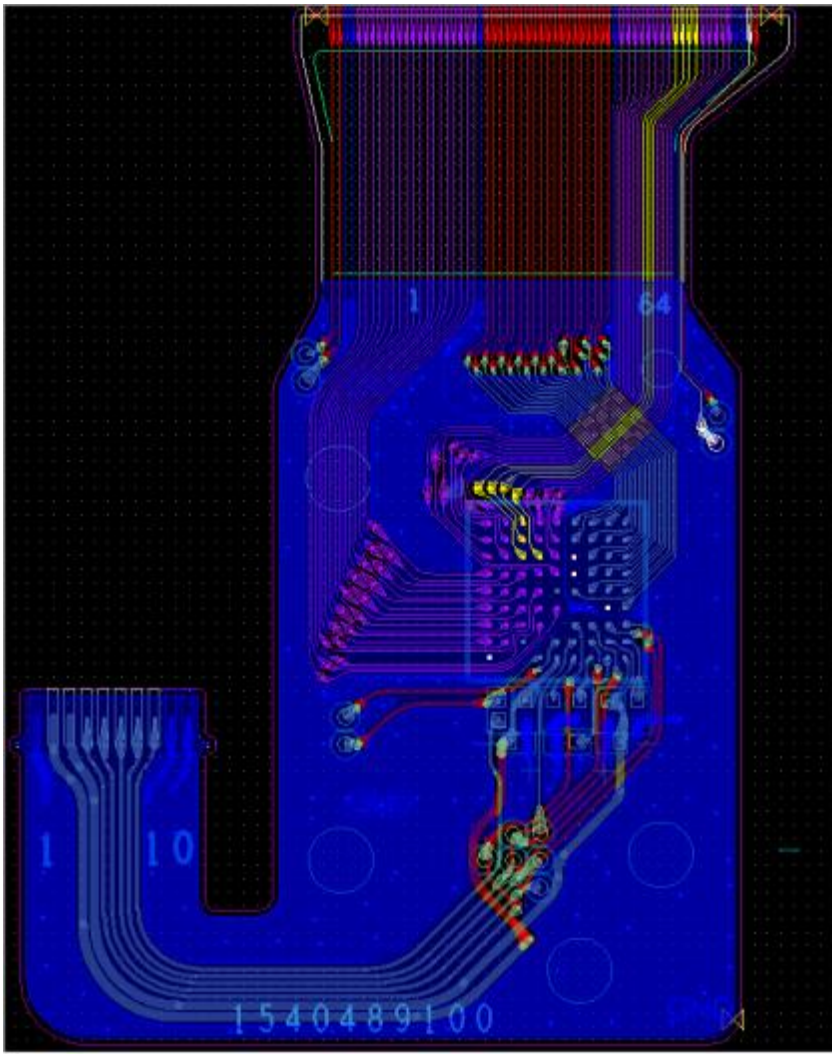


2.2 FPC layout Drawin

Main-FPC:



TP-FPC:



3 Optical Specifications

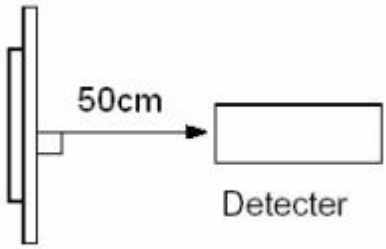
Test condition： Ta=25℃

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Luminance (with lens)		Normal mode Bp	θ=0° ϕ=0°	540	600	660	cd/m2	3.1
		HBM mode Bp	θ=0° ϕ=0°	900	1000	1100	cd/m2	
Uniformity		△Bp		80			%	3.2
Viewing Angle	Left	θL	Cr≥10	85			deg	3.3
	Right	θR		85				
	Top	ψT		85				
	Botto m	ψB		85				
Contrast Ratio		CR	θ=0° ϕ=0°	100,000			-	3.4
Color Coordinate of CIE1931	Red	x	θ=0° ϕ=0°	0.668	0.688	0.708		3.1
		y		0.291	0.31 1	0.331		
	Green	x		0.21	0.25	0.29		
		y		0.675	0.715	0.755		
	Blue	x		0.1 16	0.136	0.156		
		y		0.026	0.046	0.066		
	White	x		0.293	0.313	0.333		
		y		0.306	0.326	0.346		
Color gamut					107.16		%	3.5
Color temperature				5500	6500	7500	K	
Flicker		amount	60HZ @127Gray			-60	dB	
Color shift			θL/θR/ψT/ ψB=30°		4	5	JNCD	3.6
Lifetime			LT95		400		Hours	

3.1: Luminance measurement

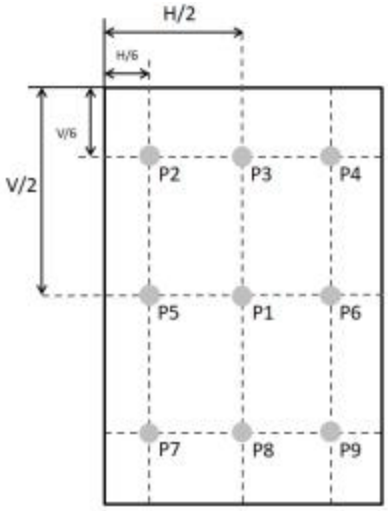
The test condition is at 25℃ and measured on the surface of OLED module.

- The data are measured after OLEDs are lighted on for more than 5 minutes and displays
- equipment PR788/CS2000/CS2000A or similar equipments (Field of view: 1deg, Distance: 50 cm)
- Measuring surroundings: Dark room.
- Adjust operating voltage to get optimum contrast at the center of the display.
- Measured value at the center point of panel must be after more than 5 minutes while light up.



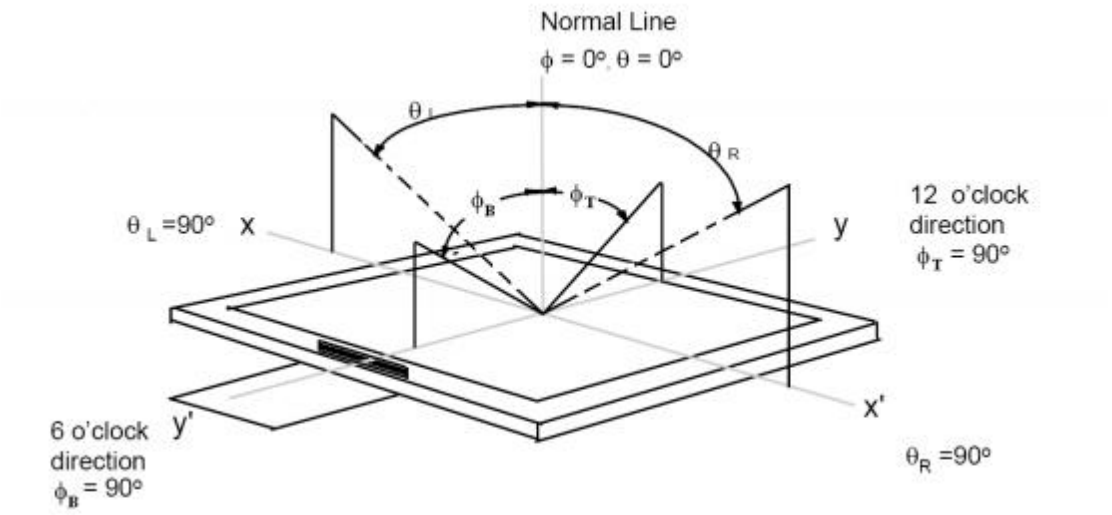
3.2: Uniformity

- The test condition is at 25℃ and measured on the surface of display module
- Measurement equipment: PR788/CS2000/CS2000A or similar equipment.
- The luminance uniformity is calculated by using following formula. △Bp = Bp (Min.) / Bp (Max.)×100 (%)
- Bp (Max.) = Maximum brightness in 9 measured spots
- Bp (Min.) = Minimum brightness in 9 measured spots.



3.3:The definition of Viewing Angle

Refer to the graph below marked by θ and Φ



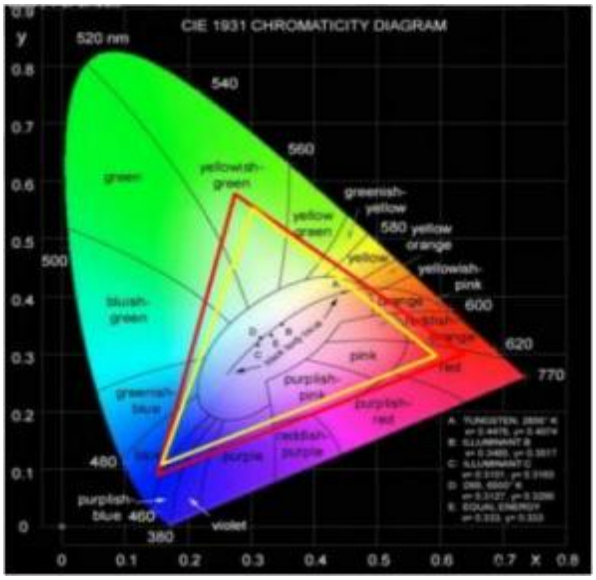
3.4: The definition of Contrast Ratio (Test OLED using PR788/CS2000/CS2000A or similar equipments):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance is at "White" state}}{\text{Luminance is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage. Black state display pure black color and luminance<0.002 nits.)

3.5: Definition of Color of CIE Coordinate and NTSC Ratio.

$$S\% = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$



3.6: Color Shift JNCD

- For JNCD measure:
- Fix on one pattern like white pattern,
- On the condition θ=0 F=0°, we can get the color coordinate (u1', v1') and on θL=30/45 °we can get another color coordinate (u2', v2')
- Delta = Square Root((u2' - u1')^2 + (v2' - v1')^2)
- For the (u', v') color space JNCD=0.0040.

4 Pin Assignments

4.1 Main FPC Pin assignment

AMOLED Interface Definition

AMOLED Pin No.	Symbol	I/O	Description
1	GND	Power	The power ground
2	GND	Power	The power ground
3	GND	Power	The power ground
4	VBAT	Power	Power IC Input Voltage
5	VBAT	Power	Power IC Input Voltage
6	VBAT	Power	Power IC Input Voltage
7	VBAT	Power	Power IC Input Voltage
8	VBAT	Power	Power IC Input Voltage
9	GND	Power	The power ground
10	VPP	Power	Power supply for OTP. Leave the pin to open when not in use
11	/		No connection
12	GND	Power	The power ground
13	D3P	I/O	MIPI DSI data3+
14	D3N	I/O	MIPI DSI data3-
15	GND	Power	The power ground
16	D0P	I/O	MIPI DSI data0+
17	D0N	I/O	MIPI DSI data0-
18	GND	Power	The power ground
19	CLKP	I	MIPI DSI clock+
20	CLKN	I	MIPI DSI clock-
21	GND	Power	The power ground
22	D1P	I/O	MIPI DSI data1+

23	D1N	I/O	MIPI DSI data1-
24	GND	Power	The power ground
25	D2P	I/O	MIPI DSI data2+
26	D2N	I/O	MIPI DSI data2-
27	GND	Power	The power ground
28	RESX	I	Thissignalwill reset thedevice andmust beapplied to properly initialize the chip. Active low.
29	VDDI	Power	Driver IC digital I/O supply
30	VCI	Power	Driver IC analog supply
31	TE	O	Tear effect output
32	GND	Power	The power ground
33	TP_VCC(2.8V)	Power	TP IC digital power supply
34	TP_VDDI(1.8V)	Power	TP IC digital I/O supply
35	TP_SDA	I/O	I2C Data Input & Output
36	TP_SCL	I/O	I2C Clock Input
37	TP_RESX	I	External Reset,Low is Active
38	TP_INT	I	Interrupt request to the host, or Wakeup request from the host.
39	ID	O	Panel ID

Note:

Module FPC connector:ZIF（39pin)：OK-F302-39115（**亚奇**）

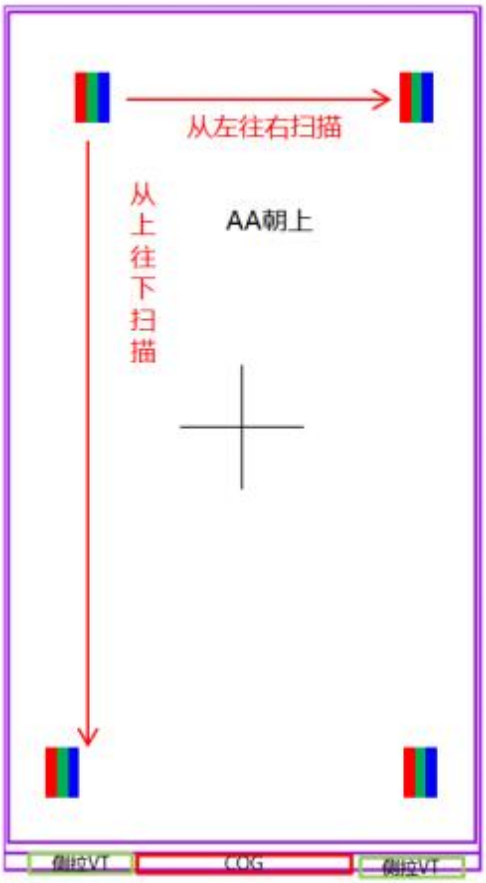
4.2 Touch FPC Pin assignment

Touch Panel Interface Definition

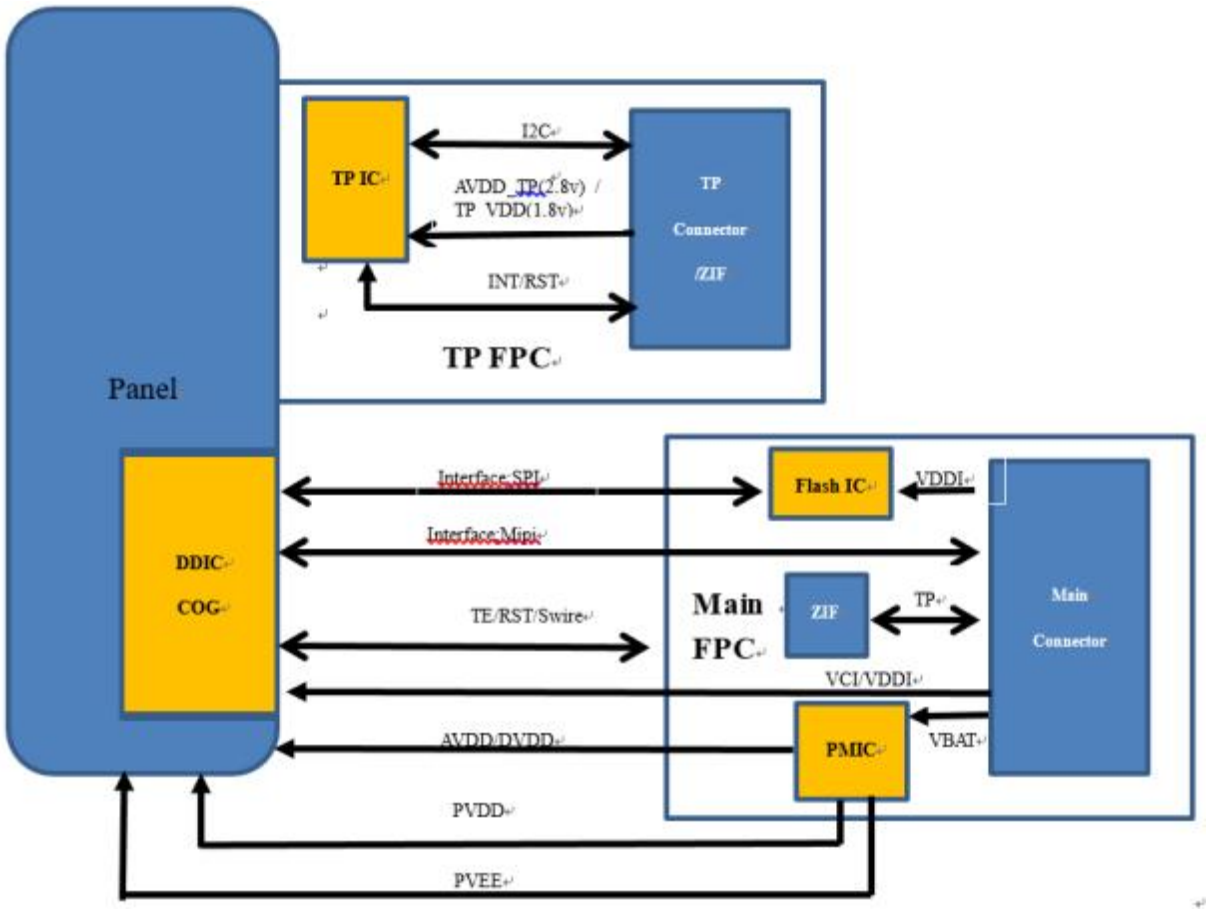
TP Pin No.	Symbol	TP Pin No.	Symbol
1	GND	7	TP_RESX
2	TP_VCC(2.8V)	8	TP_TE
3	TP_VDDI(1.8V)	9	GND
4	TP_INT	10	GND
5	TP_SDA	/	/
6	TP_SCL	/	/

5 Module Block Diagram

5.1 Graphic memory writing direction (COF 6 o' clock direction)



5.2 Module block diagram



6 Timing Characteristics

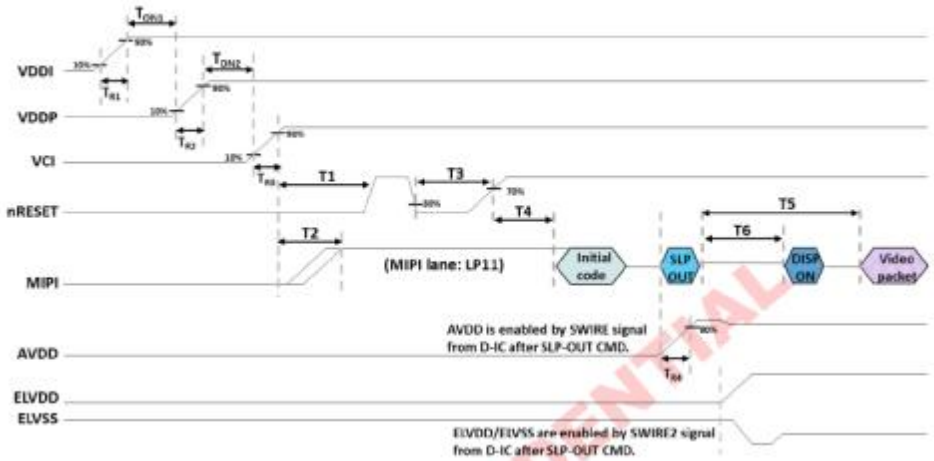
6.1 Power on/off Sequence

6.1.1 Display panel Power on/off sequence

1.Driver IC Power on sequence

Symbol	Description	Value			Unit	Note
		Min.	Typ.	Max.		
T_{ON1}	3 Power mode : VDDI on to VCI on delay 4&5 Power mode : VDDI on to VDDP or VDD on delay	> 0	-	-	ms	
T_{ON2}	4 Power mode : VDDP or VDD on to VCI on power delay time 5 Power mode : VDDP on to VDD on power delay time	> 0	-	-	ms	
T_{ON3}	VDD on to VCI on power delay time	> 0	-	-	ms	
T1	VCI on to valid to nRESET high	10	-	-	ms	
T2	VCI to MIPI bus ready delay	0	-	T1	ms	
T3	nRESET low period	50	-	-	us	
T4	nRESET high to OTP code re-load ready	15	-	-	ms	
T5	Sleep-out command received to video packet transmit delay	80	-	-	ms	
T6	Sleep-out command received to display on command transmit delay	> 0	-	-	µs	
T_{R1}	VDDI power rising time	0.1	-	2	ms	
T_{R2}	VDDP or VDD power rising time	0.1	-	2	ms	
T_{R3}	VCI power rising time	0.1	-	2	ms	
T_{R4}	AVDD power rising time	0.1	-	5	ms	

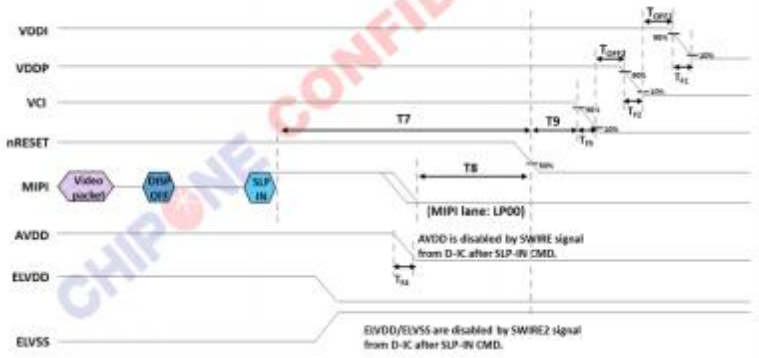
Power On Sequence for 4 Power mode #1 (EXT_DVDD_EN=0)



***Note: Unless otherwise specified, timing herein shows cross point at 50% of signal/power level. 2.Driver IC Power off sequence**

Symbol	Description	Value			Unit	Note
		Min.	Typ.	Max.		
T_{OFF1}	3 Power mode : VCI off to VDDI off delay 4&5 Power mode : VDDP or VDD off to VCI off delay	> 0	-	-	ms	
T_{OFF2}	4 Power mode : VDDP or VDD off to VDDI off delay 5 Power mode : VDD off to VDDP off delay	> 0	-	-	ms	
T_{OFF3}	VCI off to VDD off delay	> 0	-	-	ms	
T7	Sleep-in command received to valid to nRESET low	100	-	-	ms	
T8	MIPI ultra low power mode to valid to nRESET low	0	-	-	µs	
T9	nRESET low to VCI off delay	0	-	-	µs	
T_{F1}	VDDI power falling time	0.1	-	5	ms	
T_{F2}	VDDP or VDD power falling time	0.1	-	5	ms	
T_{F3}	VCI power falling time	0.1	-	5	ms	
T_{F4}	AVDD power falling time	0.1	-	5	ms	

Power Off Sequence for 4 Power mode #1 (EXT_DVDD_EN=0)



***Note:**

- Unless otherwise specified, timing herein shows cross point at 50% of signal/power level.
- Keep VGH is equal to or larger than VCI during power off sequence.

3. PMIC Startup and Shutdown Sequence

3.1 ICN67530

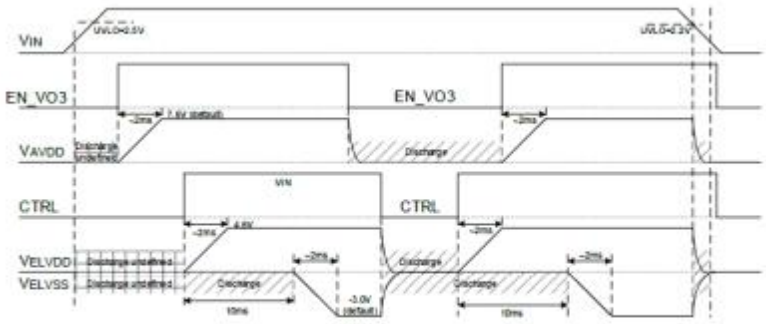


Figure 5. Start-up sequencing active discharge enabled

3.2 iML7360

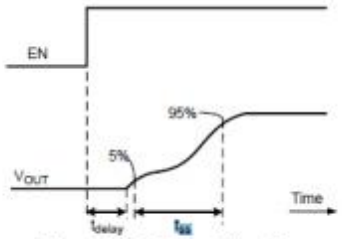


Figure 20. Soft-Start Waveform

Soft Start Period	tss		--	500	--	μs

6.1.2 TP_VCI/IOVCC at Power on/off sequence

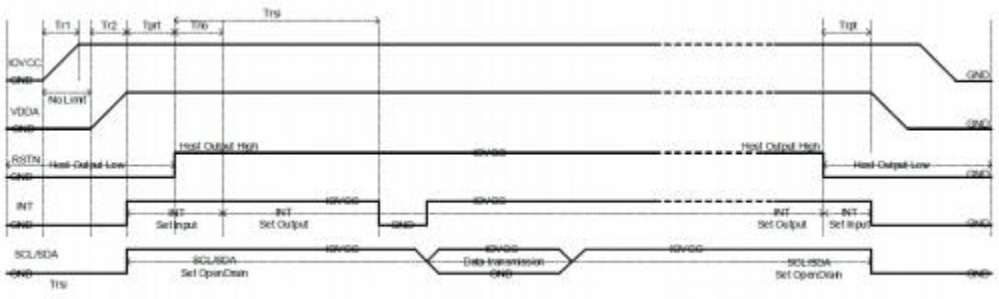


Figure 3-4-1 Power on Sequence for 2 power sources —I2C interface

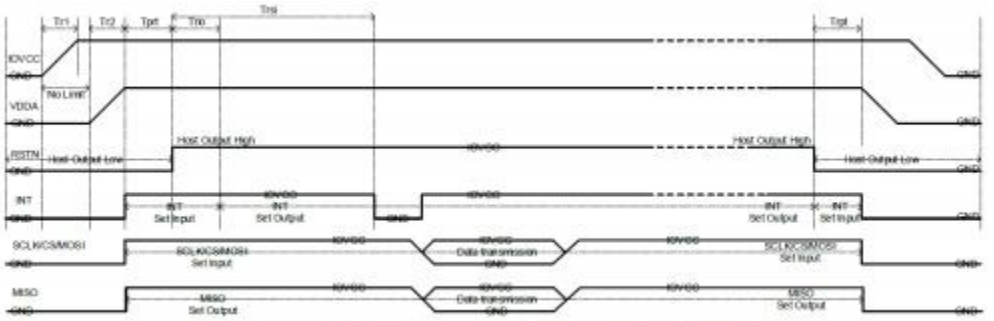
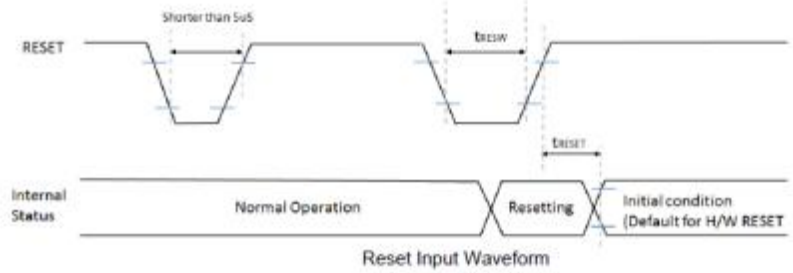


Figure 3-4-2 Power on Sequence for 2 power sources—SPI interface

6.2 Display panel reset timing

6.3 DC Characteristics for Reset



Reset Input Waveform

Parameter	Symbol	Pin	Description	MIN	TYP	MAX	Unit
Reset low pulse width	tRESW	nRESET		20	–	–	µs
Secure reset completion time	tRESET	nRESET	Reset during Sleep In mode	–	–	5	ms
		nRESET	Reset during Sleep Out mode	–	–	120	ms
Reset un-reacted pulse width		nRESET		–	–	5	µs

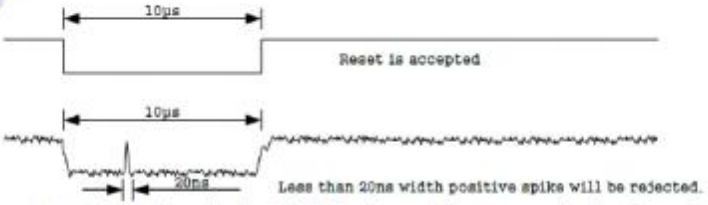
*NOTE:
1. Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table as below.

RESET Pulse	Action
Short than 5μs	Reset Rejected
Long than 20μs	Reset
Between 5μs and 20μs	Reset Start

2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

3. During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (t_{RESET}) within 5ms after a rising edge of RESET.

4. Spike Rejection also applies during a valid reset pulse as shown as below.



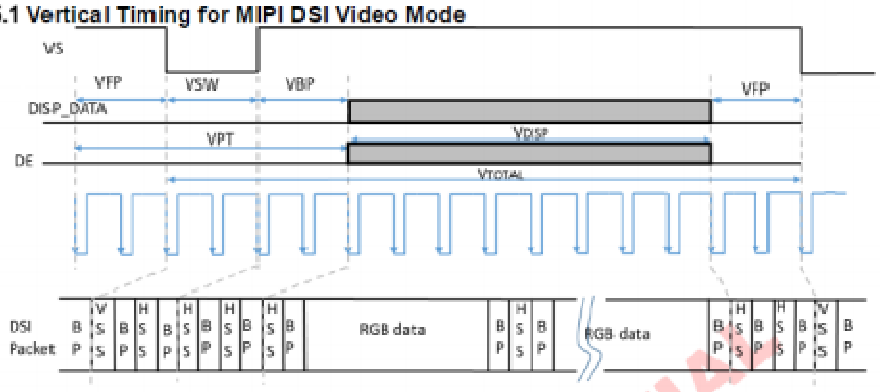
5. It is necessary to wait 5ms after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120m second.

6. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied. Internal PoR (Power-on Reset) circuit generates a reset signal within 1ms after VDDI and VCI rise up to 90% of their

6.3 Communication Interface timing

MIPI AC Timing Characteristics

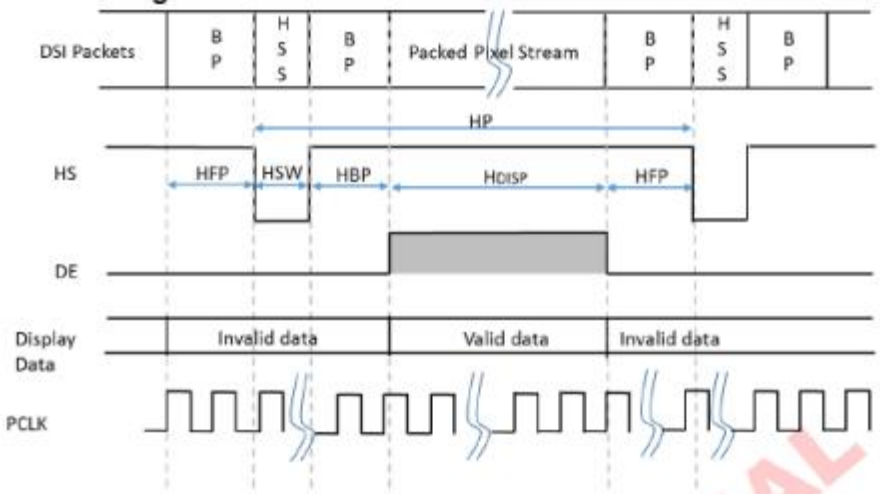
6.5.1 Vertical Timing for MIPI DSI Video Mode



Parameter	Symbol	Condition	Specification			Unit	Note
			MIN	TYP	MAX		
Vertical total	VTOTAL			TBD		Line	
Vertical low pulse width	VSW			TBD		Line	1
Vertical front porch	VFP			TBD		Line	
Vertical back porch	VBP			TBD		Line	1
Vertical data start point		VSW+VBP		TBD		Line	1
Vertical blanking period	VPT	VSW+VBP+VFP		TBD		Line	
Vertical active area	VDISP			TBD		Line	
Vertical frame rate	VFR			TBD		Hz	

*Note: The VSW and VBP pulse width are related to GOA timing. The GOA timing must be set at corresponding position for normal display.

6.5.2 Horizontal Timing for MIPI DSI Video Mode



Parameter	Symbol	Condition	Specification			Unit	Note
			MIN	TYP	MAX		
HS low pulse width	HSW			TBD		nS	
Horizontal back porch	HBP			TBD		nS	
Horizontal front porch	HFP			TBD		nS	
Horizontal data start point		HSW+HBP		TBD		nS	
Horizontal blanking period	HBLK	HSW+HBP+HFP		TBD		nS	
Horizontal active area	HDISP			TBD		nS	

7 Electrical Specifications

7.1 DC Characteristics Requirements

Parameter	Item	Symbol	Values			unit	Remark
			Min	Typ	Max		
Supply voltage (Display)	PMIC on FPC	VDDIO	1.65	1.8	3.3	V	
		VBAT	2.9	4.0	4.6	V	
Input	Input High Voltage	VIH	0.8*VDDI	-	VDDI	V	
	Input Low Voltage	VIL	VSS	-	0.2*VDDI	V	

Output	Output High Voltage	VOH IOUT = –1mA	0.8*VDDI	-	VDDI	V	
	Output Low Voltage	VOL IOUT = +1mA	VSS	-	0.2*VDDI	V	
Frame Frequency	120Hz	fFRAME	/	120	/	HZ	
	60Hz	fFRAME	/	60	/	HZ	

7.2 Power Consumption of Display and Touch

7.2.1 For Display panel

Power Supply: VDDIO= 1.8V , VCI=2.8V,Vbat=4.0V

Display Mode	Item	Typ	Max	Remark
		Power (mW)	Power (mW)	
100% Pixel On,600nits,60Hz	Normal mode	TBD	TBD	
All Pixel Off,0nits,60Hz	Normal mode	TBD	TBD	
All Pixel Off,0nits/Vci on/Vddio on	Standby mode	TBD	TBD	
10% Pixel On,100nits, 15Hz	Idle mode	TBD	TBD	
100% Pixel On,1000nits,60Hz	Boost mode	TBD	TBD	

7.2.2 For TP

Power Supply: TP_VCI=2.8V, IOVCC=1.8V

TP Report Rate: 60~120Hz adjustable @ AMOLED Frame Frequency =60Hz

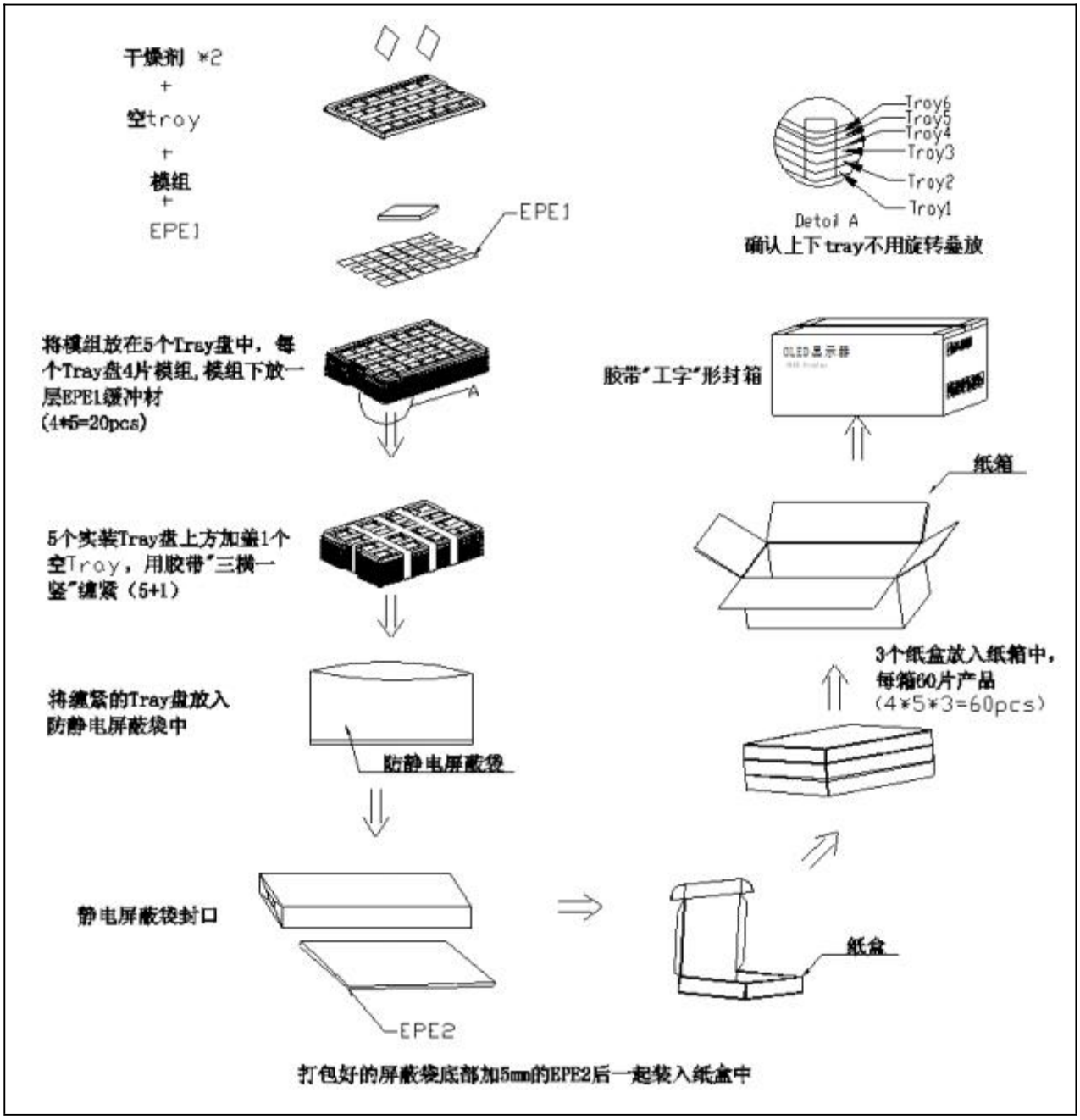
	Work Mode	Symbol	Value		Unit	Remark
			Typ	Max		
Power Consumption	Active	P	TBD	TBD	mW	
	Doze	P	TBD	TBD	mW	
	Sleep in Mode	P	TBD	TBD	uW	

8 ESD

说明： 该项测试仅针对模组贴合件进行验证。

测试项目	测试设备	测试标准	判定标准
上电空气	静电测试仪 ESS6008、静电放电枪或其他满足标准要求的设备	±4kV、±6kV、±8kV； 每个点正负各 5 次； 击打点位：lens 朝上正面 5 点	测试过程中，TP/OLED 单体受到静电脉冲干扰时，可能会出现闪屏、漏光、变暗、TP 失效等功能异常，但测试结束后，能够自动恢复正常工作
上电接触	静电测试仪 ESS6008、静电放电枪或其他满足标准要求的设备	±2kV、±4kV； 每个点正负各 5 次； 击打点位：lens 朝上正面 5 点	测试过程中，TP/OLED 单体受到静电脉冲干扰时，可能会出现闪屏、漏光、变暗、TP 失效等功能异常，但测试结束后，能够自动恢复正常工作

9 Packing


干燥剂 *2
+
空troy
+
模组
+
EPE1
EPE1
Troy6
Troy5
Troy4
Troy3
Troy2
Troy1
Detail A
确认上下 tray不用旋转叠放
将模组放在5个Tray盘中，每个Tray盘4片模组，模组下放一层EPE1缓冲材
(4*5=20pcs)
A
胶带"工字"形封箱
OLED显示器
纸箱
5个实装Tray盘上方加盖1个空Troy，用胶带"三横一竖"锁紧（5+1）
3个纸盒放入纸箱中，每箱60片产品
(4*5*3=60pcs)
将锁紧的Tray盘放入防静电屏蔽袋中
防静电屏蔽袋
静电屏蔽袋封口
纸盒
EPE2
打包好的屏蔽袋底部加5mm的EPE2后一起装入纸盒中