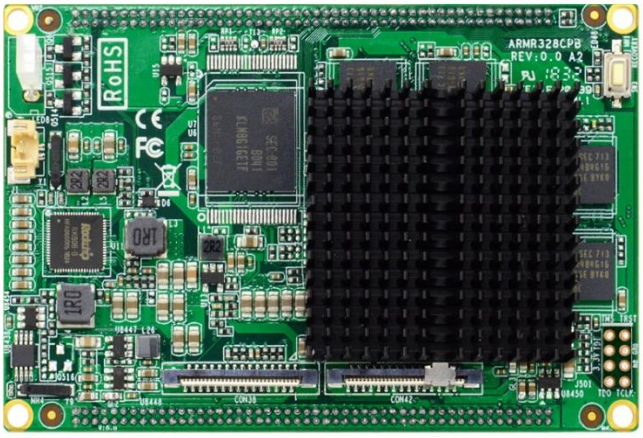
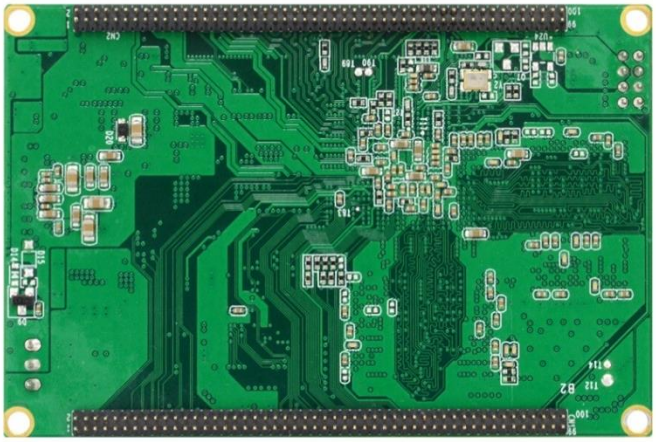
JR3288WCPB-2N

Rockchip® ARM Cortex A17 RK3288W, Core Plate Board support Extend I/O Board

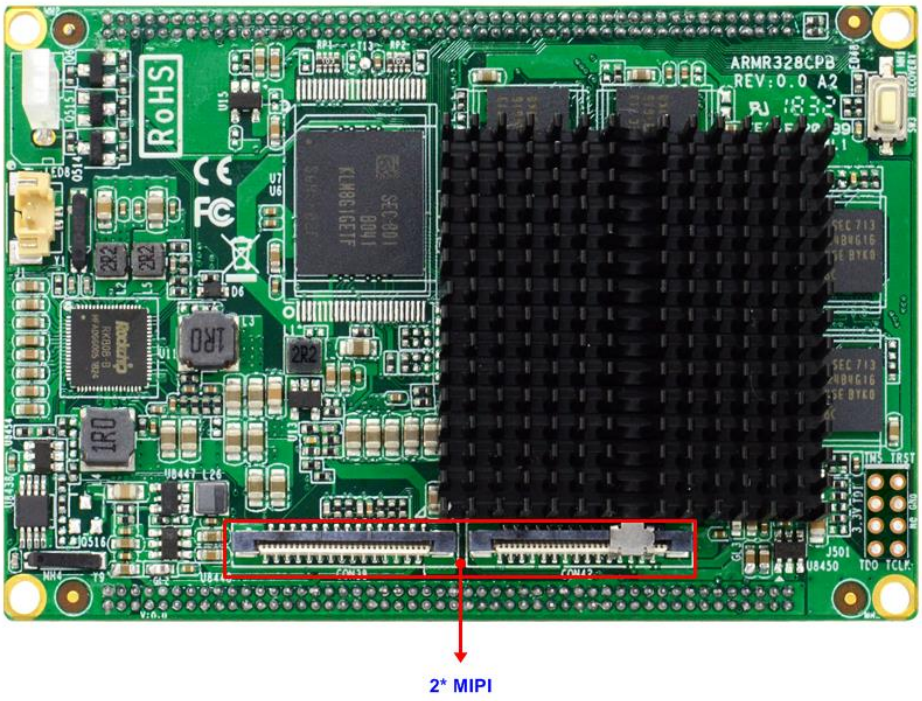


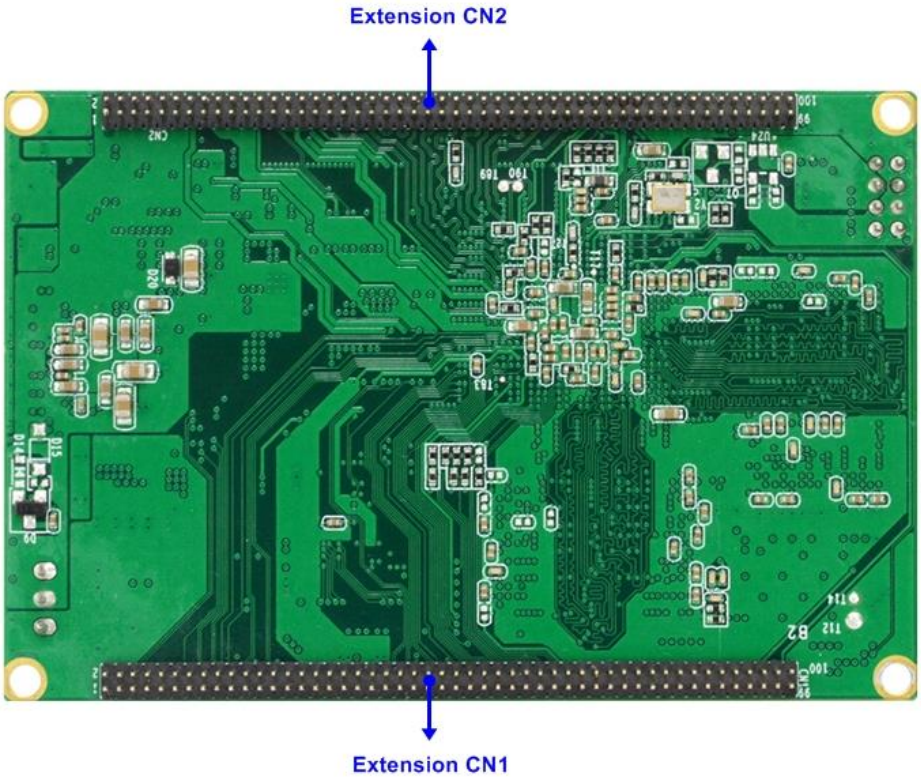


Features

1. Rockchip® ARM Cortex A17 RK3288W Quad-core 1.8GHz
2. Onboard 1333 /2GB DDR3L DRAM
3. 8G Flash ROM (Max. 32GB)
4. Support 2 * MIPI (1920 x 1080@60fps)
5. 2 * Mixture headers
6. 1.8” Form Factor (84*56mm)
7. Support Android 9.0, Linux Debian 9.0

Internal Diagram





Specifications

Model / Part Number	
Model	- JR3288WCPB-2N
Part Number	- JR3288WCPB-2N
Form Factor	
Dimensions	- 1.8” SBC (85 * 56mm, 3.35" * 2.21")
Processor System	
Processor/CPU	- Rockchip® ARM Cortex A17 RK3288W Quad-core 1.8GHz SoC Processor
GPU	- Mali-T764 GPU
Memory	
DRAM	- Onboard 2 GB DDR3L DRAM
Flash ROM	- 8GB Flash ROM (Max. 32GB)
Ethernet	
Ethernet	- By I/O Board
Wifi	- By I/O Board
3G / 4G / LTE	- By I/O Board
Graphics	
HDMI	- By I/O Board
LVDS	- By I/O Board
eDP	- By I/O Board
MIPI	- 2 (1920 x 1080@60Hz)
Multi Display	- By I/O Board
Expansion Slot	
Mini PCIe	- By I/O Board
Micro SD Socket	- By I/O Board
SIM Card Holder	- By I/O Board
Special Features	
IR Support	- By I/O Board
OS Support	- Android 9.0, Linux Debian 9.0
Watchdog Timer	- 0~255 Sec./Min. programmable
Application	- Core plate board
I/O Port	
External I/O	- By I/O Board
Internal I/O	- 2* Mixture Headers
Power Requirements	
Input PWR	12V DC-in - AT : Directly PWR on as Power input ready

	- ATX : Press Button to PWR on after Power input ready
Certifications	
Certifications	- RoHS, CE, FCC, CE-LVD
Environment	
Temperature	- Operating: -10°C ~ 60°C with 0.7 m/s air flow - Storage: -20°C ~ 70°C
OS Support	
OS Support	- Android 9.0, Linux Debian 9.0
Warranty	
Warranty	- 2 Years Limited Warranty

*Specifications subject to change without notice, not responsible for typographical errors. Does not include HDD or OS.

OS Support List

SKU	Android	Linux
RK3128	5.1	
RK3288	9.0	Debian 9.0
RK3328	7.1	
RK3399	7.1	Debian 9.0

Extension Function Header Pin Define

CN1 (100Pin)

PIN	PIN definition	Default function	PIN	PIN definition	Default function
1	GND	GND	2	HDMI_HPD	HDMI Hot Plug Detection interrupt
3	32KOUT2	32.768KHz clock output, for wifi	4	TX2+	HDMI channel 2 differential serial data positive
5	PWR_EN	IR power control input	6	TX2-	HDMI channel 2 differential serial data negative
7	PMIC_PWRON	power button ,active low	8	TX1+	HDMI channel 1 differential serial data positive
9	SLEEP_INT	Sleep mode control input	10	TX1-	HDMI channel 1 differential serial data negative
11	RESET	RESET	12	TX0+	HDMI channel 0 differential serial data positive
13	HDMI_CEC	HDMI CEC communication	14	TX0-	HDMI channel 0 differential serial data negative
15	I2C5_SDA_HDMI	I2C serial port 5,for HDMI	16	TXC+	HDMI differential pixel clock positive
17	I2C5_SCL_HDMI	I2C serial port 5,for HDMI	18	TXC-	HDMI differential pixel clock negative

19	I2S_SCLK	I2S port, for audio part	20	EDPAUXP	eDP differential AUX channel positive output
21	I2S_LRCK_RX	I2S port, for audio part	22	EDPAUXN	eDP differential AUX channel negative output
23	I2S_LRCK_TX	I2S port, for audio part	24	EDPTX3P	eDP differential lane 3 positive output
25	I2S_SDI	I2S port, for audio part	26	EDPTX3N	eDP differential lane 3 negative output
27	I2S_SDO0	I2S port, for audio part	28	EDPTX2P	eDP differential lane 2 positive output
29	I2S_MCLK	I2S port, for audio part	30	EDPTX2N	eDP differential lane 2 negative output
31	I2C2_SDA	I2C serial port 2,for Audio	32	EDPTX1P	eDP differential lane 1 positive output
33	I2C2_SCL	I2C serial port 2,for Audio	34	EDPTX1N	eDP differential lane 1 negative output
35	UART0_RX	UART0 serial port, for BT module	36	EDPTX0P	eDP differential lane 0 positive output
37	UART0_TX	UART0 serial port, for BT module	38	EDPTX0N	eDP differential lane 0 negative output
39	UART0_CTS	UART0 serial port, for BT module	40	EMMC_CLKO	EMMC clock out
41	UART0_RTS	UART0 serial port, for BT module	42	SDMMC_D0	SDMMC0 data port
43	SDIO0_D0	SDIO0 data port, for WIFI module	44	SDMMC_D1	SDMMC0 data port
45	SDIO0_D1	SDIO0 data port, for WIFI module	46	SDMMC_D2	SDMMC0 data port
47	SDIO0_D2	SDIO0 data port, for WIFI module	48	SDMMC_D3	SDMMC0 data port
49	SDIO0_D3	SDIO0 data port, for WIFI module	50	SDMMC_CLK	SDMMC0 clock output
51	SDIO0_CMD	SDIO0 command output, for WIFI module	52	SDMMC_CMD	SDMMC0 command output
53	SDIO0_CLK	SDIO0 clock output, for WIFI module	54	SDMMC_DET	SDMMC0 detect input
55	BT_WAKE	CPU wake up BT module	56	UART1_RX	UART1 serial port
57	WIFI_REG_ON	WIFI module internal regulators power enable output	58	UART1_TX	UART1 serial port
59	BT_RST	BT module reset output	60	UART4_CTS	UART4 serial port
61	WIFI_HOST_WAKE	WIFI module wake up CPU	62	UART4_RTS	UART4 serial port
63	BT_HOST_WAKE	BT module wake up CPU	64	UART4_TX	UART4 serial port
65	PHY_TXD2	MAC transmit data	66	UART4_RX	UART4 serial port
67	PHY_TXD3	MAC transmit data	68	4G_PWR	4G module power enable output
69	MAC_RXD2	MAC receive data	70	4G_RESIN_N	4G module RESET
71	MAC_RXD3	MAC receive data	72	12V_EN	12V enable output
73	PHY_TXD0	MAC transmit data	74	IR_INT	Infrared Radiation signal receive
75	PHY_TXD1	MAC transmit data	76	DC5V_EN	DC5VIN power enable output
77	MAC_RXD0	MAC receive data	78	OTG_VBUS_DRV	USB OTG power control output
79	MAC_RXD1	MAC receive data	80	LED2_CTL	PS2_DATA/GPIO8_A1

81	MAC_MDC	MAC management clock	82	CABC_EN	Lvds PWM enable
83	MAC_RXDV	MAC receive data valid	84	LED_EN	Lvds panel backlight enable output
85	MAC_CLK	MAC reference clock output	86	LCD_RST	mipi_lvds reset
87	PHY_TXEN	MAC transmit enable	88	SPK_CTL	Amplifier Shutdown mode control input
89	MAC_MDIO	MAC management command and data	90	UART3_RX	UART3 serial port
91	MAC_RXCLK	MAC receive clock	92	UART3_TX	UART3 serial port
93	PHY_RST	MAC RESET	94	GPIO7_B3	GPIO7_B3
95	PHY_TXCLK	MAC transmit clock	96	GPIO7_B6	UART1 5v power enable output
97	CON28_USB_PWR	USB power enable output	98	I2C1_SDA	I2C1_SDA
99	GND	GND	100	I2C1_SCL	I2C1_SCL

CN2 (100Pin)

PIN	PIN definition	Default function	PIN	PIN definition	Default function
1	GND	GND	2	VCC_SYS	Input voltage 5V
3	VCCIO_WL	APIO3 digital IO power supply 1.8V	4	VCC_SYS	Input voltage 5V
5	VCCIO_WL	APIO3 digital IO power supply 1.8V	6	VCC_SYS	Input voltage 5V
7	VCC_18	Output voltage 1.8V	8	VCC_SYS	Input voltage 5V
9	VCC_18	Output voltage 1.8V	10	VCC_SYS	Input voltage 5V
11	VCCA_18	Output voltage 1.8V for Audio	12	VCC_SYS	Input voltage 5V
13	VCCIO_SD	Output voltage 3.3V For SDMMC0_VDD	14	VCC_SYS	Input voltage 5V
15	VCC18_LCD	Output voltage 1.8V for EDP/LVDS/HDMI/MIPI	16	VCC_IO	Output voltage 3.3V
17	VCC18_LCD	Output voltage 1.8V for EDP/LVDS/HDMI/MIPI	18	VCC_IO	Output voltage 3.3V
19	VCC_SD	TF CARD power supply 3.3V	20	VCC_IO	Output voltage 3.3V
21	VCC_SD	TF CARD power supply 3.3V	22	VCC_IO	Output voltage 3.3V
23	VCC_LAN	Output Ethernet power 3.3V	24	CIF_PDN0	Camera power down control output
25	VCC_LAN	Output Ethernet power 3.3V	26	CIF_CLKOUT0	Camera clock output
27	VCCA_33	Output voltage 3.3V for APIO4_VDD/LVDS_AVDD_3V3/Audio	28	VDD18_CAM	MIPI-DSI/CSI power supply Input 1.8V
29	VCCA_33	Output voltage 3.3V for APIO4_VDD/LVDS_AVDD_3V3/Audio	30	VDD18_CAM	MIPI-DSI/CSI power supply Input 1.8V
31	LVDS_CLK1P	LVDS differential clock lane 2 positive	32	MIPI_TX/RX_D0P	MIPI-DSI/CSI differential lane 0 positive
33	LVDS_CLK1N	LVDS differential clock lane 2 negative	34	MIPI_TX/RX_D0N	MIPI-DSI/CSI differential lane 0 negative

35	LVDS_D8P	LVDS data port	36	MIPI_TX/RX_D1P	MIPI-DSI/CSI differential lane 1 positive
37	LVDS_D8N	LVDS data port	38	MIPI_TX/RX_D1N	MIPI-DSI/CSI differential lane 1 negative
39	LVDS_D7P	LVDS data port	40	MIPI_TX/RX_CLKP	MIPI-DSI/CSI differential clock lane positive
41	LVDS_D7N	LVDS data port	42	MIPI_TX/RX_CLKN	MIPI-DSI/CSI differential clock lane negative
43	LVDS_D6P	LVDS data port	44	MIPI_TX/RX_D2P	MIPI-DSI/CSI differential lane 2 positive
45	LVDS_D6N	LVDS data port	46	MIPI_TX/RX_D2N	MIPI-DSI/CSI differential lane 2 negative
47	LVDS_D5P	LVDS data port	48	MIPI_TX/RX_D3P	MIPI-DSI/CSI differential lane 3 positive
49	LVDS_D5N	LVDS data port	50	MIPI_TX/RX_D3N	MIPI-DSI/CSI differential lane 3 negative
51	LVDS_CLK0P	LVDS differential clock lane 1 positive	52	MIPI_TX_D0P	MIPI_LVDS data port
53	LVDS_CLK0N	LVDS differential clock lane 1 negative	54	MIPI_TX_D0N	MIPI_LVDS data port
55	LVDS_D3P	LVDS data port	56	MIPI_TX_D1P	MIPI_LVDS data port
57	LVDS_D3N	LVDS data port	58	MIPI_TX_D1N	MIPI_LVDS data port
59	LVDS_D2P	LVDS data port	60	MIPI_TX_CLKP	MIPI_LVDS differential clock lane positive
61	LVDS_D2N	LVDS data port	62	MIPI_TX_CLKN	MIPI_LVDS differential clock lane negative
63	LVDS_D1P	LVDS data port	64	MIPI_TX_D2P	MIPI_LVDS data port
65	LVDS_D1N	LVDS data port	66	MIPI_TX_D2N	MIPI_LVDS data port
67	LVDS_D0P	LVDS data port	68	MIPI_TX_D3P	MIPI_LVDS data port
69	LVDS_D0N	LVDS data port	70	MIPI_TX_D3N	MIPI_LVDS data port
71	I2C3_SDA	I2C serial port 3,for camera	72	I2C3_SCL	I2C serial port 3,for camera
73	AD_IN0	Battery voltage input	74	AD_IN2	GPS VTUNE ADC input
75	DVP_PWR	Camera power enable output	76	HPMIC_DET	Audio detect output
77	PHY_PMEB	PHY power management event	78	IR_DET	Mic detectT output
79	ARM_WOKING	ARM_WOKING	80	PHY_INT	PHY interrupt output
81	UART2_TX	Uart2 serial port data output for debug	82	CODEC_INT	Audio interrupt output
83	UART2_RX	Uart2 serial port data input for debug	84	GPIO7_B4	GPIO7_B4
85	I2C4_SDA	I2C4_SDA	86	I2C4_SCL	I2C4_SCL

87	LCD_ADJ	LCD panel backlight brightness control output	88	GPIO7_B5	GPIO7_B5
89	CON29_USB_PWR	USB power enable output	90	LED1_CTL	SC_DET/GPIO8_A2
91	CON30_USB_PWR	USB power enable output	92	OTG_ID	USB OTG ID detect input
93	OTG_DET	USB OTG connected detect input	94	OTG_DP	USB OTG Data Plus port
95	4G_USB_DP	USB HOST2 Data Plus port for 4G module	96	OTG_DM	USB OTG Data Minus port
97	4G_USB_DM	USB HOST2 Data Minus port for 4G module	98	HOST1_DP	USB HOST1 Data Plus port
99	GND	GND	100	HOST1_DM	USB HOST1 Data Minus port

Standard Accessories

Part Number	Description
	JR3288WCPB-2N

Mechanical Drawings (Unit = mm)