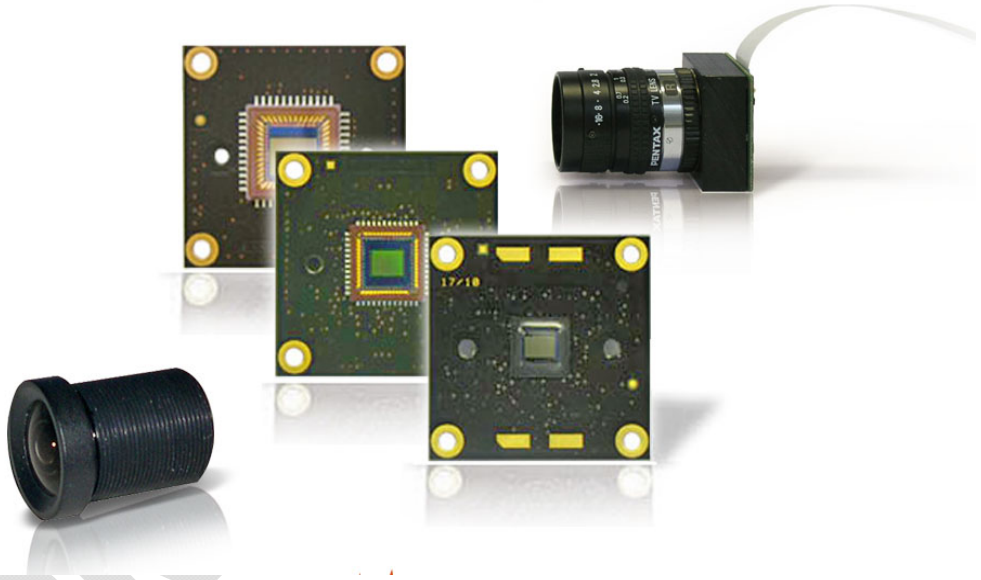
phyCAM-P / phyCAM-S

Embedded Camera Modules



Manual

10th Edition

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10th Edition

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Revision History

Rev.No.	Changes	Changed by	Issue Date
1	Initial Release	M. Klahr	01.03.2010
2	VM-009, VM-010 added	M. Klahr	12.05.2011
3	VM-008 added, phyCAM-S+ spec. added	M. Klahr	10.02.2012
4	skipped (not available)	-	-
5	VM-011 added, minor changes	M. Klahr	25.02.2013
6	VM-011 added section “variable resolution”	M. Klahr	07.03.2013
7	VM-011 Electrical Specification: Clock Frequency corrected	D. Bender	03.06.2013

8	Section 3.2.3.2: added flip-type connector changes in sections: 2.2.4, 2.2.5, 3.2.4 sections added: 4.2.5.1, 4.5.5.1, 5.2.3.1, 5.5.3.1 minor changes in technical data	D. Bender	12.11.2013
9	VM-012 added	M. Klahr	23.01.2015
10	VM-010 / VM-010-LVDS: updated to PCB-version PL1331.4 VM-011 / VM-011-LVDS: updated to PCB-version PL1331.4 PL1372.1 VM-012: J1 changed from PL1420.1 VM-012: Figure66, Figure 90 changed Design Guide updated Changed sensor manufacutrer name Aptina to On Semiconductor	M. Klahr	03.06.2016

1 Introduction

phyCAM digital camera modules are designed to bring image processing into embedded microprocessor designs. Together with PHYTEC System on Modules (SOM) subassemblies, phyCAMs offer an easy and efficient way to add imaging capabilities to an embedded application.

phyCAM camera modules directly connect to the digital camera interface on PHYTEC SOMs. Many BSPs for PHYTEC SOMs already include appropriate software drivers for phyCAM digital camera modules. This enables easy deployment of phyCAMs into customer end products. The phyCAM interface specification is open, allowing phyCAMs to be used with other microprocessors or hardware designs in addition to PHYTEC SOMs.

The interface definition of the each phyCAM family is identical for all products within each family. Thus, several different camera modules can be connected to the same target hardware circuitry. This allows the system designer to interchange phyCAM camera modules during the design phase of the product as well as to enable update of camera modules without the need to redesign target hardware circuitry.

The phyCAM consists of two basic interface families, both of which allow easy integration into and adaptation to a particular application's requirements:

- phyCAM-P
- phyCAM-S

Both interface systems are described in detail in this manual.

A wide range of powerful 32-bit microprocessors are supported by the phyCAM, including the Marvell PXA series, Freescale i.MX processors and the Texas Instruments OMAP family. Together with the numerous variants of phyCAM camera modules, embedded developers can choose an optimal combination of microprocessors and camera modules for a given project.

Each phyCAM is available either as bare PCB version or with lens holders for C/CS-Mount or M12-lenses. This enables phyCAM modules to be easily integrated into target systems (also referred to in this manual as target hardware application modules) according to both optical and mechanical requirements.

1.1 The phyCAM – Interface Concepts

phyCAMs are available in two basic interface families:

- phyCAM-P – parallel data bus
- phyCAM-S – serial LVDS data connection

The characteristics of the data bus type must be considered in regards to target hardware system design, driving selection of the appropriate architecture: phyCAM-P or phyCAM-S.

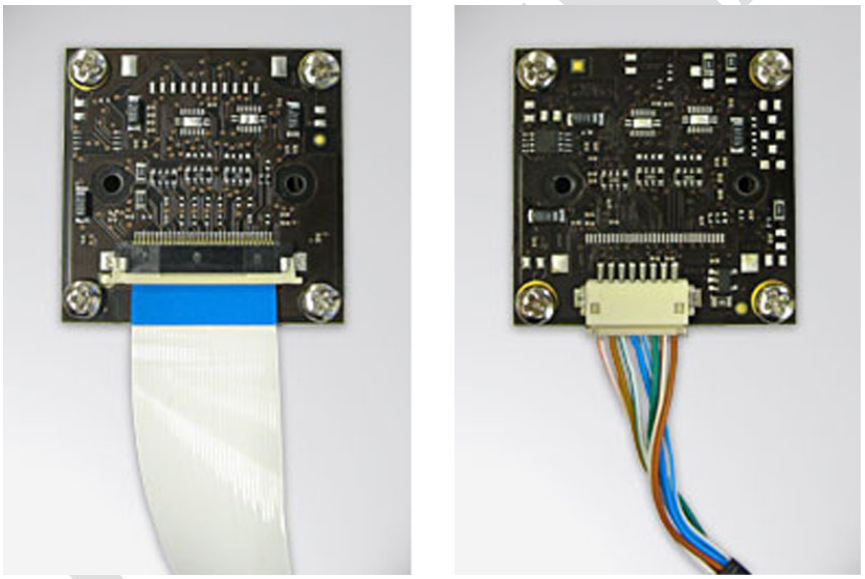


Figure1: phyCAM-P (on the left) and phyCAM-S interface (on the right)

The phyCAM - regardless of the interface type - routes the following signals between the camera and microprocessor:

- Camera power supply
- Camera master clock
- Camera image data
- I²C control bus for camera configuration
- Special function signals (phyCAM-P only)

The following sections describe the most important properties of the two interface types:

1.1.1 phyCAM-P

The parallel version of the phyCAM offers a very easy and cost-efficient way to integrate a camera into an application.

Data and control signals are transmitted via a 33-pin FFC cable. This reduces components needed for the interface to a minimum while maintaining compatibility between camera modules within the phyCAM-P parallel family. Reserved pins allow the use of special functions of the camera module, such as a trigger input or LED light control.

Image data can be transmitted with up to 10-bit color or grey scale resolution (color depth per each color channel).

The phyCAM-P is especially suitable for applications in which the camera is installed within device housing. The maximum cable length is specified as 30 cm.

The phyCAM-P interface fits seamlessly to phyCORE System on Modules. Additionally, some phyFLEX modules feature a parallel camera interface as an optional secondary camera.

1.1.2 phyCAM-S

The phyCAM-S uses a serial LVDS interface for the transmission of data and clock signals. Accordingly, the phyCAM-S data interface consists of only 8 signals, including power supply and control signals.

The advantages of this interface system are:

- More options for laying cable inside a device housing. Simple twisted pair wires can be used for routing of LVDS signals, which results in very flexible cabling options. The camera modules are populated with compact, Hirose headers, which allow fast and easy interfacing to cable connectors. The differential signal lines have robust EMI characteristics, which is advantageous for longer camera cables.
- Support of up to 5 meter cable length. This enables separation of the camera module “head” from the main system “body”. For external connection, a simple CAT-5e cable or RJ-45 port can be used.
- A standardized voltage level of the data lines, resulting in design simplicity and ensuring the interchangeability of different camera modules.

phyCAM-S camera modules interface to PHYTEC’s phyCARD and phyFLEX family System on Modules. All SOMs in these families offer the corresponding LVDS camera interface. Similar to the scalability of the phyCAM, embedded engineers also benefit from the flexibility, scalability and interchangeability of these SOMs.

Characteristics of LVDS

LVDS (Low Voltage Differential Signaling) is an interface standard for fast data transmission. LVDS is standardized according to ANSI/TIA/EIA-644-1995. This norm defines the physical layer, but not the protocol layers that are based on it.

The most important features of LVDS are:

- Differential voltage levels
- Relatively low voltage levels
- Signals are provided by a constant current source
- Data is typically transmitted serially

LVDS works with a voltage swing of 0.3 V. The logic level is represented by the differential voltage level of two leads - the

differential pair - rather than by the absolute level referred to Ground. A logic shift is created by reversing polarity of the lines. The absolute voltage level referred to Ground is 1.2 V, while the differential voltage is only 0.3 V. This results in robust EMI characteristics.

This combination of low voltage signaling and high signal frequencies requires careful PCB layout. Differential pair wires should be twisted. However, for short distances a parallel cable design, such as a flat-band ribbon cable, is possible.

Most of the common camera interfaces are parallel rather than LVDS. Because of this, a deserializer is needed at the processor-side circuitry. This deserializer converts the incoming data stream from the camera to a parallel interface with asymmetrical voltage levels (referenced to Ground). Accordingly, the clock signal fed to the camera is converted to an LVDS signal by an LVDS driver. PHYTEC phyCARD and phyFLEX series SOMs are already populated with a deserializer. This enables easy connection of phyCAM-S cameras to phyCARDs.

1.2 Overview of the phyCAM features

*) if the module features an additional parallel camera interface (optional)

Table 1 shows the key features for selecting either phyCAM-P or phyCAM-S for a given application:

Feature	phyCAM-P	phyCAM-S
Cost effective design	+	
Cable length > 30 cm		+
Camera types shall be interchangeable	+	++
More than 8-bit color depth per channel required	+	
Flexible cable required		+
Use of special camera features	+	
Detached camera design		+
High data rate	+	
Most robust EMI characteristics		+
Use with phyCORE family SOM	+	
Use with phyCARD family SOM		+
Use with phyFLEX family SOM	+ *)	++

*) if the module features an additional parallel camera interface (optional)

Table 1: Selection Guide: phyCAM-P / phyCAM-S

In general, phyCAM-P allows simple interface design requiring minimal circuitry and components, allowing easy and cost-effective development of a custom, target hardware application board in support of a phyCAM-P camera module. Depending on the microprocessor, respective PHYTEC SOM, and camera module used in an application, a simple one-by-one wiring of the camera interface is sufficient.
In case the camera and processor have different voltage levels, level shifters might be needed to adapt the camera signals to the processor. In order to support camera interchangeability, adaptive-level translation is required.

The interface circuitry of standard PHYTEC Carrier Boards can also be used as a reference and departure point for design of target hardware for a given application. *Section 6* provides reference circuitry for such target hardware supporting phyCAM-P and phyCAM-S camera modules.

The phyCAM-P features dedicated control lines, which support individualized selection of additional features of the parallel camera

module. Typical features are trigger- and strobe signals or a selection signal for the I²C address range of the camera. Some phyCAM-P modules offer several different functions which can be selected by jumpers on the camera module PCB. PHYTEC offers customized camera module configurations for projects involving volume phyCAM deployment.

Please note that the function of additional feature pins may vary between the different phyCAMs. If the use of several camera modules is intended, please assure that utilized feature pins are compatible.

In contrast, the phyCAM-S offers a fully standardized interface. Besides pin assignment, the signal level of all pins is defined. To use a different camera module, simply load the appropriate software driver and the other camera is ready for use. Any additional features of the camera are not transferred through the interface cable. Instead, such additional function signals are available through an auxiliary connector on the respective camera module.

phyCAM-S designs are slightly more complex because of the components needed for LVDS transmission, level shifting of the control signals and power supply. However, the phyCAM-S offers a more flexible design, even more robust EMI characteristics than the phyCAM-P, and extended cable length support.

Please note that phyCARD and phyFLEX SOMs already feature the LVDS deserializer, thus simplifying the design of application target hardware.

Note:
Please contact PHYTEC to discuss selection of the appropriate phyCAM interface for your application.

1.3 Mechanical and Optical Connection

The mechanical and optical integration of the camera in a device depends on several factors. The phyCAM embodies a modular system

that addresses various design considerations:

- **Mounting**
  All phyCAMs provide identical mounting options. Each camera module has six attachment points: four on the outer edges of the camera and two in the middle, next to the sensor. The latter can be supplied visually covered.

- **Mechanical**
  The mechanical dimensions are likewise identical, enabling interchangeability of phyCAM camera modules. Please see the section 2 - *Specifications* - for dimensional drawings of phyCAM camera modules.

- **Optical**
  In regards to optical connections, phyCAMs support different camera sizes as well as lens quality and design.

Each camera module is available in the following configurations:

- **M12 – Lens holder**
  In this version, the camera module is equipped with a holder for M12 lenses, also known as D-Mount. An M12 lens holder is also included in PHYTEC Embedded Video Kits. M12 lenses provide a reasonable compromise between size and lens quality. They are available in many focal lengths and aperture variations. The four holes on the PCB edge can be used for mounting the camera module.

- **C/CS-Mount – Lens holder**
  This lens holder provides a good solution for applications that have high to very high demands regarding the quality of image reproduction. The lens holder is made of plastic with a metal thread insert. This allows the precise adjustment of back focus. Both C and CS mount lenses can be used. For C-mount lenses, an optional adapter ring (PHYTEC part #: AZ008) must be inserted between lens and camera. The camera module is mounted onto the plastic housing with four screws. C/CS mount lenses offer excellent picture quality. Options such as adjustable aperture and zoom or telecentric design are available.

- **PCB version**
  This option offers maximum freedom to the developer. The camera module can be used together with special lens holders or can be integrated directly into device housing. The PCB version is suitable for special applications, such as laser technology. All six attachment points can be used for mounting. Optionally, the board can be shipped with the inner mounting holes covered by light-proof material.

Figure2: Housing options: M12, C/CS-Mount, PCB (with samples of lenses)

1.4 Typical Design Flow

With phyCAMs and various processor SOMs, PHYTEC offers unique modular Embedded Imaging Kit systems to the designers of custom hardware. The standardized phyCAM interface allows the

combination of components that best fit the requirements of a given application.

The development of a customized embedded imaging system with integrated camera has six basic steps:

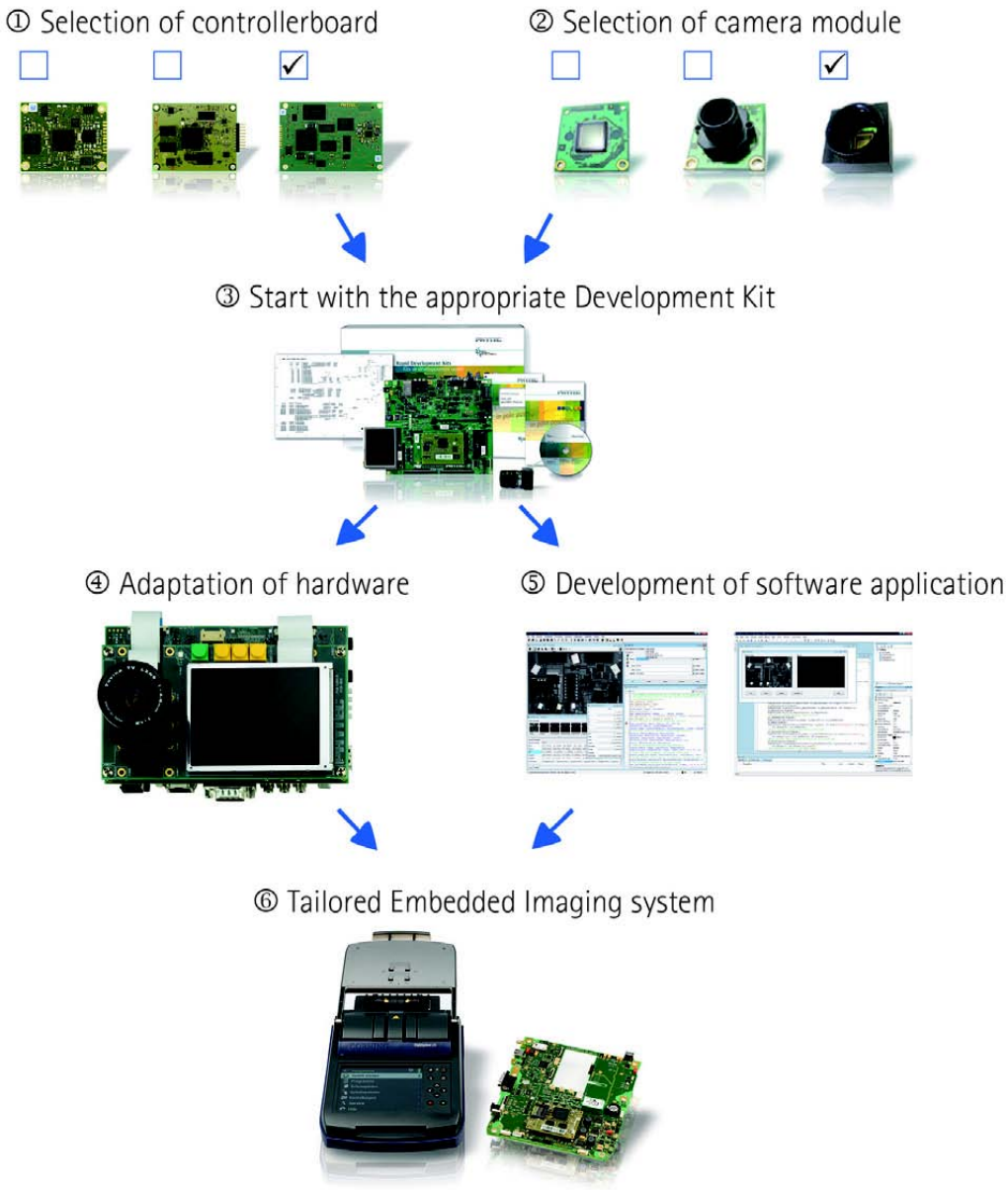


Figure3: Typical Design Flow

1. *Selection of the appropriate microprocessor-based SOM*
   PHYTEC offers a wide variety of 32-bit SOMs supporting many different features. PHYTEC digital imaging hardware supports phyCORE, phyCARD and phyFLEX product lines.

2. *Selection of the Camera module*
   The PHYTEC digital imaging product line includes monochrome (b/w) and color sensor cameras at various resolutions and color (data-) formats. Each camera module is available in three mechanical variations. In respect to the specification of the project, the developer can choose between a plain PCB version as well as either a M12 lens holder or a C/CS-mount lens holder. PHYTEC also offers adapters for capturing signals of analog video cameras (video digitizer module, part # VM-008).

3. *Start with a PHYTEC Embedded Imaging Development Kit*
   The development kit contains a System on Module, camera module, standard Carrier Board and all required cables. In addition, each kit contains an applicable software Board Support Package (BSP) including necessary drivers for the camera module. These kit contents enable development of embedded imaging application software independent from, and even in advance of, customized application hardware.

4. *Application Hardware*
   The Carrier Board included in the kit, as well as the accompanying schematics, serves as a reference design for development of a customized target hardware application board. Since all complex microprocessor circuitry is on the SOM, design of a customized application board is easy. PHYTEC offers support for design of target hardware. PHYTEC can also be contracted do the customized hardware design for our customers.

5. *Development of Application Software*
   Development of application software can be performed in parallel with the hardware design, starting with use of the Kit. This saves valuable development time. PHYTEC also

provides complex image processing libraries that are already supported in the BSPs.

For example, the HALCON Embedded image processing software, Open CV library or other imaging libraries can be used to integrate predefined algorithms into application code.

6. *End Product*
   Due to use of various off-shelf PHYTEC SOMs and camera modules, customized end user hardware and software can be developed within minimal time. Use of off-shelf PHYTEC solutions also significantly reduces design risk, as development of custom target hardware application modules is less complex than design of complete microprocessor circuitry of the SOM. Additionally, appropriate design of hardware and software makes it possible to scale camera features and processing power by interchanging SOMs and camera modules.

2 Specifications

2.1 Specifications of the phyCAM-P Interface

Main characteristics of the interface:

- Parallel image data transfer from the camera to the microprocessor
- Parameterization of the camera through an I²C communication bus
- 33-pin FFC-connector 0.5mm pitch, cable thickness 0.3 mm
- Operation and signal voltage levels depend on the camera sensor used on the camera module. The level translation is done on the PHYTEC Carrier Board or, if necessary, on the customized target hardware application board. The camera interface offers automatic detection of the required voltage level through a resistive setup pin
- Recommended cable length < 30 cm

Interface signals:

- Power supply to the camera
- Master clock to the camera
- Image data and sync signals from the camera
- I²C–bus for camera control and – if available– additional functions on the camera module
- Control signals (optional: reset, output enable, ...)
- Additional functions (optional: trigger, strobe, I/O-signals, …)

2.1.1 Connector

33-pin FFC/FPC, 0.5 mm pitch, 0.3 mm thick, contact position bottom

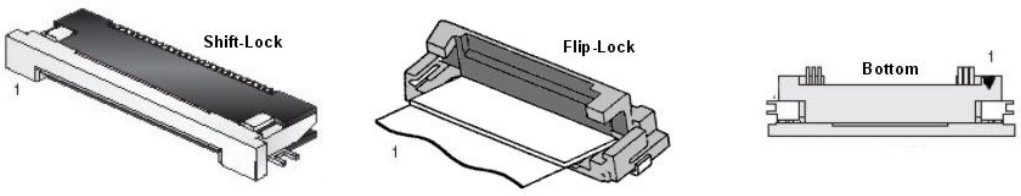


Figure4: FFC-connector phyCAM-P (left: top view, right: solder side, example)

Matching cables:

Length	Contact type	PHYTEC part #
120 mm	A	WF062
200 mm	A	WF043
300 mm	A	WF046

Contact type A: contacts are located on the same side of the cable

2.1.2 phyCAM-P – Interface Pin Assignment

Pin assignment of the camera module:

phyCAM-P - Electrical Interface (33-pin FCC connector)			
Pin	**Dir.**	**Name**	**Function**
1	PWR	Vcam	Power Supply Input
2		Vcam	
3	I	CAM_RST	Reset Signal (optional – refer to camera description)
4	-	GND	Ground
5	I/O	CAM_SDA	SDA, I²C-Interface
6	I	CAM_SCL	SCL, I²C-Interface
7	I/O	CAM_CTRL1	Camera Dependent Feature (Addr. Sel.,Trigger, I/O…)
8	-	GND	Ground
9	O	CAM_FV	VSYNC
10	O	CAM_LV	HSYNC
11	-	GND	Ground
12	OUT	CAM_DD9	D9
13	OUT	CAM_DD8	D8
14	-	GND	Ground
15	OUT	CAM_DD7	D7
16	OUT	CAM_DD6	D6
17	-	GND	Ground
18	OUT	CAM_DD5	D5
19	OUT	CAM_DD4	D4
20	-	GND	Ground
21	OUT	CAM_DD3	D3
22	OUT	CAM_DD2	D2
23	-	GND	Ground
24	OUT	CAM_DD1	D1
25	OUT	CAM_DD0	D0
26	-	GND	Ground
27	O	CAM_PCLK	Pixel Clock
28	-	GND	Ground
29	I	CAM_MCLK	Master Clock
30	I/O	CAM_CTRL2	Camera Dependent Feature2 (Addr. Sel.,Trigger, I/O…)
31	O	Power Voltage Set	Resistor to GND. Sets Supply and Signal Voltage Level
32	I	CAM_OE	Data Lines Output Enable (optional)
33	PWR	Vcam	Power Supply Input

Notes: PWR=Power, I=Input, O=Output, with respect to the camera

Table 2: Pin Assignment phyCAM-P - Interface

Notes:

- The supply voltage V_{CAM} can be different for various camera modules. Please refer to the detailed descriptions of specific phyCAMs. Carrier Boards that support multiple phyCAM modules must be equipped with an adaptive power supply. Reading the resistance value of pin 31 detects the appropriate voltage of the Carrier Board and automatically configures the voltage regulator.

- Signal levels on the data- and control lines depend on the camera module in use. Reading the resistance value of pin 31 detects the appropriate voltage of the Carrier Board. Carrier Boards that support multiple phyCAM modules must be populated with level shifters to adapt the signal levels to the microprocessor utilized in the design. Please see the circuitry references in section 6.1.

- The signal levels of the I²C interface are consistent with the levels of the data lines. Each I²C bus requires pull-up-resistors on both SDA and SCL lines. Pull-up resistors must be installed on the Carrier Board unless they already populate the SOM.

- Depending on the camera chip on the phyCAM, the functions of the control pins CAM_CTRL1 / CAM_CTRL2 can vary. In standard configuration these pins are configured as inputs and should be left open or connected via a jumper (GND / V_{CAM}) to Ground by a 200 Ω series resistor.
  Default setting: GND.

  For CAM_CTRL1 the default function of the pin is address select for the I²C interface, if supported by the camera sensor. CAM_CTRL2 is used as an additional Ground connection per default function. If the camera supports other functions on this pin, ensure that this does not conflict with the default setting.

- Signal direction of the sync lines FV, LV und PCLK is “out”. This means that the camera controls the camera interface of the microprocessor. This is called “master mode”. If the camera

also supports slave mode, these signals can also be configured as inputs. However, this is an optional configuration and does not have to be considered when designing a custom target hardware application board.

- The control signal CAM_OE sets the data- and, optionally, also the sync lines (FV, LV und PCLK) into tri state mode if supported by the camera sensor. This feature is optional. For more information please refer to the camera sensor specification. The CAM_OE pin is not required for application board design. If not needed, this pin should be left open. This will enable the data- and sync lines.

Note:
The pin numbers refer to the connector on the camera module. Please note that depending on the cable and FFC connectors used, the pin numbering on the target hardware application board might be mirrored.

2.1.3 Voltage Selection – Resistor

Pin 31 of the camera connector supports the voltage setting for the camera on the target hardware application board. On the camera module this pin is connected to Ground (GND) by a dedicated resistor. The resistor value, measured at Pin 31 relative to GND, specifies the supply voltage of the operating voltage and the data lines of the camera module. This enables the target hardware to automatically adapt to the required signal level.

The following table defines the resistor values and the corresponding operating and signal voltages:

Voltage Selection	
V_{CAM} and signal level	**Resistance at pin 31 with respect to GND**
3.3 V	0 Ω
2.8 V	220 Ω
1.8 V	1720 Ω

tolerance: +/- 4%

Table 3: Voltage-Selection - Resistor

Note:
The resistance values are defined in a way that they can be used as Ground-end resistors in the feedback path of the variable voltage regulator. Please see section 6.1.2 for examples.

2.2 Specification of the phyCAM-S Interface

Main characteristics of the interface:

- Image data, clock and sync signals of the camera are transferred by a serial LVDS interface to the processor interface.
- Parameterization of the camera, as well as access to the camera configuration registers, via I²C bus
- 8-pin miniature crimping connector, 1.25 mm pitch.
- 3.3V operating voltage and signal level of the I²C interface
- Recommended maximum cable length: 6 m. (using a CAT-5e cable. The maximum length is depending on cable type and quality.)

Interface signals:

- Power supply (3.3V) to the camera
- Master clock to the camera (LVDS)
- Image data and sync signals from the camera (LVDS)
- I²C interface for camera control and – if available – additional functions on the camera module

2.2.1 Connector

8-pin Hirose miniature 1.25 mm pitch crimping connector.
Connector type on the camera module: Hirose DF13A-8P-1.25H (PHYTEC part #: VM205)

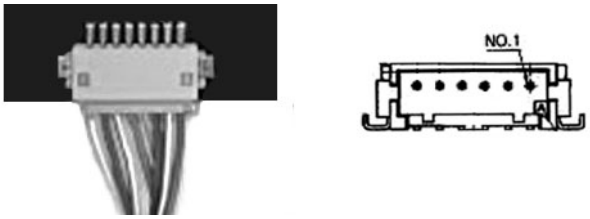


Figure5: phyCAM-S connector

Mating sockets for cable manufacturing:

- Hirose DF13-8S-1.25C (single row socket)
- Hirose DF13-2630SCFA (crimping contact for AWG 26...30)

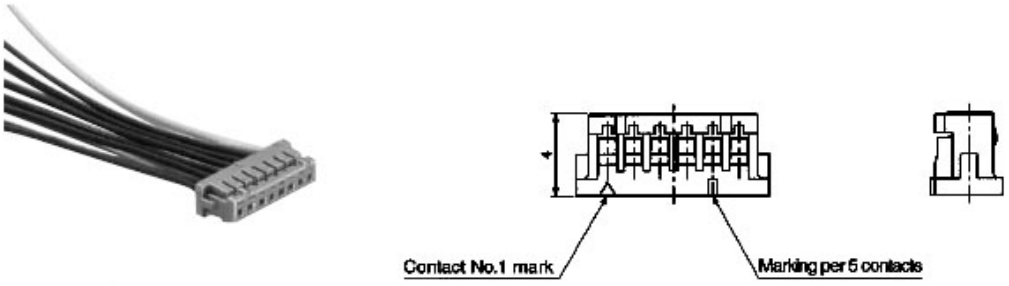


Figure6: phyCAM-S Cable Socket

Please note that twisted pair wires are strongly recommended for the differential pairs of the LVDS signal lines. The cable impedance should be 100 Ω.

PHYTEC uses CAT-5 or CAT-7 cables for external wiring (cable outside a device's housing). These cables types are also included in PHYTEC development kits. These cables terminate in a Hirose connector on the Carrier Board side, and terminate in an RJ-45 (8P8C) connector on the target hardware application board side.

2.2.2 phyCAM-S – Interface Pin Assignment

Pin assignment of the camera module:

phyCAM-S - Electrical Interface Camera module (Hirose DF13A-8P-1.25H)			
Pin	**Signal**	**Dir**	**Description**
1	LVDS DATA P	OUT	LVDS data from camera
2	LVDS DATA N	OUT	
3	LVDS CLOCK N	IN	Master clock to camera
4	SDA	I/O	I²C-interface, data line (3.3V signal level)
5	SCL	IN	I²C-interface, clock line (3.3V signal level)
6	LVDS CLOCK P	IN	Master clock to camera
7	VCC +3,3V	IN	3.3V supply voltage, 300 mA max.
8	GND	-	Ground connection

Signal direction with respect to the camera

Table 4: Pin Assignment of the phyCAM-S – Interface (Hirose-connector)

When using a Hirose connector, it is recommended to use the same pin assignment at the target hardware application board side.

To connect the phyCAM-S to the Carrier Board, PHYTEC uses a RJ-45 connector. This allows the connection of camera module with a CAT-5 Cable. The maximum cable length is 6 m (depending on cable type and quality).

Pin assignment of the RJ-45 connector

phyCAM-S - Electrical Interface RJ-45 (8P8C)			
Pin	**Signal**	**Dir**	**Description**
1	LVDS DATA P	IN	LVDS data from camera
2	LVDS DATA N	IN	
3	LVDS CLOCK N	OUT	Master clock to camera
4	SDA	I/O	I²C-interface, data line (3.3V signal level)
5	SCL	OUT	I²C-interface, clock line (3.3V signal level)
6	LVDS CLOCK P	OUT	Master clock to camera
7	VCC +3.3V	OUT	3.3V supply voltage, 300 mA max.
8	GND	-	Ground connection

Signal direction with respect to the Carrier Board

Table 5: Pin Assignment of the phyCAM-S – Interface (RJ-45 connector)

Notes:

- LVDS DATA: Image data and sync signals from the camera as a serial LVDS data stream. Usually data has to be deserialized on the target hardware application board or the SOM.

phyCARD SOMs already provide an internal deserializer. See section 2.2.3 for more information about data formats.

- LVDS CLOCK: Master clock to the camera as LVDS signal. The target hardware application board has to be equipped with a corresponding LVDS driver. See section 6.2 for a reference design.

- Supply voltage: +3.3V (+3.0V…+3.6V)
  The target hardware application board must supply the camera module. Maximum current draw is approximately 300 mA. PHYTEC recommends allowing for higher current consumption for future camera models. Note that long cables might cause significant voltage drop.

- SCL/SDA: I²C interface for configuration of the camera and – if available - additional functions of the camera module. The camera acts as an I²C slave. The I²C voltage level is 3.3V. Each I²C bus requires pull-up-resistors on both SDA and SCL lines. Pull-up resistors must be installed on the target hardware application board. When using long camera cables voltage drop on the I²C lines to the camera must be taken into consideration when selection the pull-up resistors. Note that if I²C buffers or line drivers are used on the application board the high level / low level input voltages might have different levels than standard I²C devices.

2.2.3 Data Format on the LVDS line

Image data is transferred from the camera as a 10-bit serial data stream with 8-bits pixel data and 2-bits sync signals (*Line Valid* and *Frame Valid*).

Data Bit LVDS	Function
D0	Image Data D0
D1	Image Data D1
D2	Image Data D2
D3	Image Data D3
D4	Image Data D4
D5	Image Data D5
D6	Image Data D6
D7	Image Data D7

D8	Line Valid (LV)
D9	Frame Valid (FV)

Table 6: phyCAM-S LVDS Data Bits Assignment

Note:

- The information carried by the data bits depends on the camera sensor used on the camera module. For example, when using a monochrome sensor, D[0..7] can represent brightness information per pixel. When using a color sensor, information will be sequential raw pixel data in Bayer-Pattern (RGB format) or processed color information (RGB or YUV format). Please see the specification of the camera model.
- Pixel clock is transferred as an embedded signal in the LVDS stream. It is recovered by the LVDS deserializer.

2.2.4 Electrical Characteristics phyCAM-S Interface

Table 7 shows the electrical characteristics of the receiver side (Carrier Board) of the phyCAM-S interface. Cameras connected to a phyCAM-S receiver should match these parameters.

	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CAM}	3.0	3.3	3.6	V
LVDS-Deserializer					
PCLK Frequency	f_{PCLK}	16	-	40	MHz
Reference Clock Duty Cycle	-	-	50	-	%
Differential Threshold High Voltage	VTH	-	+15	-	mV
Differential Threshold Low Voltage	VTL	-	-15	-	mV
Input Current	I_{IN}	-20	±1	+20	µA
Shunt	R_{SHUNT}		100		Ω
LVDS-Driver (MCLK)					
MCLK frequency	f_{MCLK}	-	-	200	MHz
Differential output voltage	$\|V_{OD}\|$	-	350	-	mV
Impedance	-		100		Ω

Table 7: Electrical Characteristics phyCAM-S Interface

Important:

- PCLK must be applied continuously. This means that no dropouts may occur at the pixel clock line. Otherwise, the LVDS transceivers will not lock to the signal.
- During power-up the supply voltage must rise strictly increasing. Otherwise the internal reset circuits of the camera module might not work correctly. This might result in no data output on the LVDS interface.

2.2.5 Electrical Characteristics phyCAM-S+ Interface

The phyCAM-S+ interface is an improvement of the phyCAM-S interface in regards to maximum pixel clock frequency. phyCAM-S+ is capable of transmitting camera signals with a pixel clock (*PCLK)* frequency up to 80 MHz

The phyCAM-S+ is electrically compatible to the phyCAM-S interface.

A phyCAM-S camera can connect to a SOM via a phyCAM-S+ interface if the minimum clock frequency of *PCLK* is higher than 20 MHz

phyCAM-S+ cameras can connect to a SOM via a phyCAM-S interface if the maximum *PCLK* frequency is lower than 40 MHz.

	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CAM}	3.0	3.3	3.6	V
LVDS-Deserializer					
PCLK Frequency	f_{PCLK}	20	-	80	MHz
Reference Clock Duty Cycle	-	-	50	-	%
Differential Threshold High Voltage	VTH	-	+15	-	mV
Differential Threshold Low Voltage	VTL	-	-15	-	mV
Input Current	I_{IN}	-20	±1	+20	µA
Shunt	R_{SHUNT}		100		Ω
LVDS-Driver (MCLK)					
MCLK frequency	f_{MCLK}	-	-	200	MHz
Differential output voltage	$\|V_{OD}\|$	-	350	-	mV
Impedance	-		100		Ω

Table 8: Electrical Characteristics phyCAM-S+ Interface

Important:

- PCLK must be applied continuously. This means that no dropouts may occur at the pixel clock line. Otherwise, the LVDS transceivers will not lock to the signal.
- During power-up the supply voltage must rise strictly increasing. Otherwise the internal reset circuits of the camera module might not work correctly. This might result in no data output on the LVDS interface.

2.3 Mechanical Specifications

Tolerances:
PCB dimensions: ±0.25 mm
Drill holes: ±0.1 mm
Plastic components: ±0.5 mm

All information is subject to change.

2.3.1 Camera PCB Dimensions

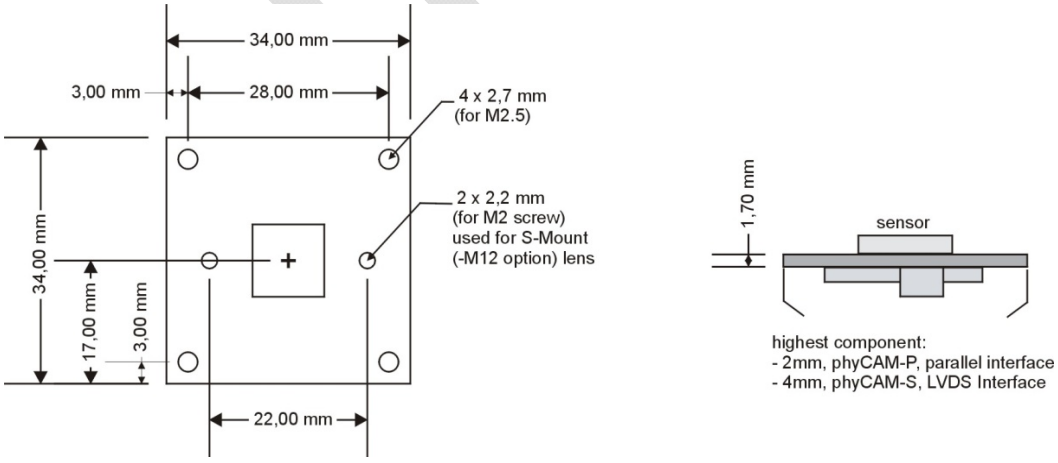


Figure7: phyCAM Printed Circuit Board (PCB) Dimensions

The cable outlet is located on top side in relation to the standard sensor readout direction.

The outer mounting holes are surrounded by a metalized area of 5mm in diameter. Screw heads, washers or other mounting elements are allowed within this area. The inner mounting holes are surrounded by a non-conducting (not metalized) area of 4.5mm in diameter. If mounting elements are larger than these areas, use non conductive materials to prevent short circuits between conductive components. Please note that the position of electrical components on the camera modules is subject to change.

On request, the camera modules can be shipped with the inner mounting holes (2.2 mm dimensions) covered with intransparent material. Please note that the plugs providing the covering have a profile of approx. 2.5 mm on the sensor side of the camera.
The connector for trigger/strobe signals has a height of 4.9 mm (installed only if camera module supports this feature).

Note:
Since optical lenses flip the image vertically (upside down), camera modules are usually mounted with the cable outlet located on the bottom side. Many camera sensors allow reverting the readout direction via software. Therefore other mounting positions are also possible.

2.3.2 Dimensions with C/CS-Mount lens holder

Camera modules with a C/CS-mount lens holder are denoted by the suffix –H in the PHYTEC part number.

The lens holder is equipped with a brass ring for precise adjustment of the back focal distance. The lens holder can be secured by a set screw. For using C-Mount type lenses with the camera module, an additional adapter ring is screwed on top of the lens holder (PHYTEC part #: AZ008).

One side of the holder is equipped with threaded holes for mounting. The holder can be mounted either with four M2.5 screws or with one ¼" photo screw.

In standard configuration, the cable outlet points towards the mounting holes. However, the camera module can be turned in increments of 90° so that mounting is possible from any side.

Lens holder material: polyoxymethylene (POM, Delrin), black
C/CS mount threat insert ring: Brass

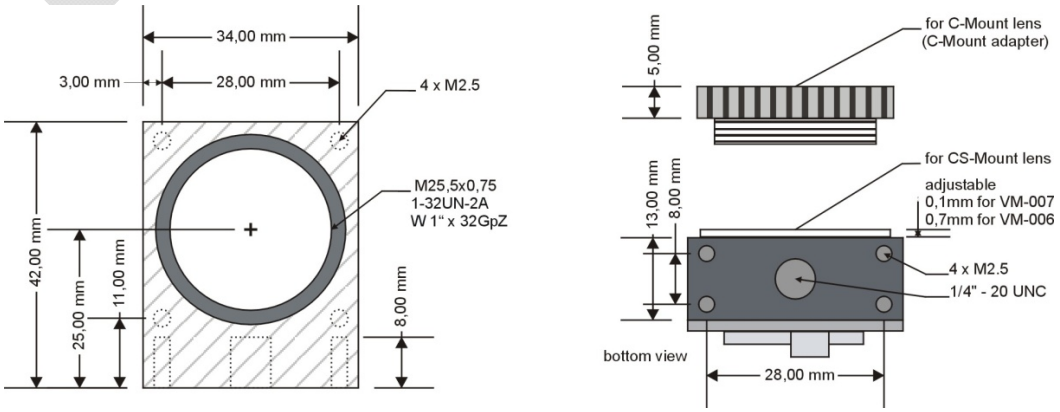


Figure8: Dimensions phyCAM with C/CS-Mount Lens Holder

2.3.3 Dimensions with M12 Lens Holder

Camera modules with a lens holder for M12 / 0.5 lenses (S-Mount) are denoted by the suffix –M12 in the PHYTEC part number.

The holder mounts on the camera PCB by two M2 screws using the inner 2.2 mm holes of the board. The camera module can be mounted using the four 2.7 mm mounting holes. Screws with a diameter of 2.5 mm are recommended for mounting the camera module.

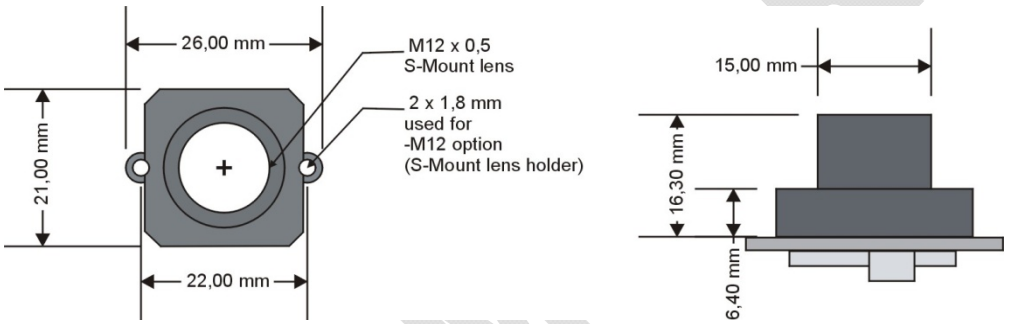


Figure9: phyCAM Dimensions with M12 lens holder

3 Getting Started with PHYTEC Development Kits

PHYTEC offers ready-made, off-shelf development kits for various combinations of SOMs and camera modules. These kits are an ideal basis for evaluating phyCAM hardware and software. The kits accelerate the design process by supporting development and test of application software in advance of development of target hardware.

The kits can also be used for test of additional hardware components in advance of development of final application board target hardware, as the Carrier Board included in the kits offers an expansion bus to connect to additional, peripheral hardware components. Such testing reduces design risks during the development and prototyping phase, as well as allows the adaption, development and testing of the software for any such additional hardware components.

Note:
If a desired processor/camera module combination is not available as a kit, we recommend starting with a kit that is the best match to the desired configuration. This allows familiarization with kit contents as well as programming environment. As a next step, connect the desired camera module, which is not available in a pre-packaged kit, to the standard kit Carrier Board. Please note that additional cameras have to be ordered separately.

Please contact PHYTEC for consulting regarding the best design process for a project.

3.1 Development Kit Start Up

We recommend that kit users familiarize themselves with the basic functions of the kit and the development software before evaluating the camera and image processing components. Each kit comes with QuickStart Instructions that guide the user through the kit installation process and offer examples on how to use the software tools included in the kits.

3.2 Setting up the Camera

3.2.1 Software Requirements

Note:
The sections below explain the approach for both Linux and Windows CE operation systems. Please note that there might be slight differences in the details of these approaches, depending on the OS / kernel version.

3.2.1.1 Embedded Linux

phyCAM digital camera modules are supported by the appropriate camera drivers included in the PHYTEC Linux BSP for specific SOMs. The list of supported of new camera modules is continuously expanding. Please check the driver folder of the current kernel version to determine which devices are supported by a given BSP. The path to the driver folder is kernel version dependent and appears as follows:

../lib/modules/<Kernel_Version>/kernel/drivers/media/video/…

The name of a camera driver always refers to the model of the camera sensor used on the phyCAM camera module. If camera modules are backward compatible, the previous driver name will be used.

Examples:

phyCAM Camera module	Driver Name
VM-006-series (Aptina MT9M001-sensor)	mt9m001
VM-007-series (Aptina MT9V022-sensor)	mt9v022
VM-009-series (Aptina MT9M131-sensor)	mt9m111
VM-010-series (Aptina MT9V024-sensor)	mt9v022
VM-011-Serie (Aptina MT9P031/006-Sensor)	mt9p031

More information about the camera sensor characteristics can be found in the technical specifications of the camera modules *(chapter 4)*.

Application software has direct access to the cameras by the *Video4Linux 2* – interface (V4L2). Multimedia frameworks like

GStreamer can also access the camera driver using the V4L2 interface. Use *Capability Querying* to determine the set of V4L2 functions supported by specific camera drivers. This mechanism, as well as the description of the functions, is explained in the V4L2 instructions. Please see *video for Linux Two API Specification*.

GStreamer is a tool to quickly test certain camera functions and display a camera image. *GStreamer* can easily be configured by editing scripts. Kits include readymade scripts that use GStreamer to display the camera image on the display, as well as to transfer image streams to another computer, or store images in various data formats.

The scripts also show how to expand Gstreamer examples by accessing camera registers. The desired configuration is defined by editing a text file. Simply select or deselect predefined register configurations. Additional individual edits and extensions to the file are also possible. Read the *LAN-052 "AppNote_Set_Cam_Register"* application note to learn more about this feature.

Depending on your module and the BSP version additional demo software and examples are available, for example:

- …\v4l2_c-examples\...
  (C-code to demonstrate access to the V4L2 interface)
- …\opencv_examples\...
  (Access to the V4L2 camera interface from OpenCV)
- …\gstreamer_examples\tools\...
  (Reading and writing the camera settings via the I²C - Bus)

3.2.1.2 Windows CE 6.0

phyCAM digital camera modules are supported by the appropriate camera drivers included in the Windows Embedded CE BSP for applicable SOMs.

The list of supported of new camera modules is continuously expanding. Call the function *Start/Settings/Control Panel/SelCamera* to view a list of currently supported camera models. Please refer to

section 3.2.4.2 “Starting the Windows Embedded CE Demo” to learn how to test a camera connected to a kit Carrier Board.

The interface of the camera drivers is compatible to *DirectShow*. The demo software included in Development Kits show how to access the camera driver. This can also be used as a reference for user application software.

The demo software includes the following basic functions:

- Live view of an image on the display
- Live image freeze
- Save a snapshot as a BMP file
- Save a snapshot as a raw file
- Read from and write to individual registers of the camera sensor.

Depending on the camera module, additional functions - such as color correction for the color models - might be available.

The desired configuration is defined by editing a text file. Simply select or deselect predefined register configurations. Additional individual edits and extensions to the file are also possible. Please read the application note *LAN-052” AppNote_Set_Cam_Register”* to learn more about this feature.

3.2.2 Hardware Requirements

The following components are required to start-up the camera. Note that PHYTEC Embedded Imaging Kits already contain the following required components:

- Standard PHYTEC Development Kit: SOM, Carrier Board, LCD, other relevant components
- phyCAM camera module, including a lens and lens holder
- Connection cable from the camera to the Carrier Board.

For users who already have a standard - rather than Embedded Imaging - Development Kit, please note that:

- most PHYTEC Development Kits can be upgraded to Embedded Imaging Kits if a phyCAM-S/ phyCAM-P interface is available on the standard kit Carrier Board
- Additional cameras can be added to an Embedded Imaging Kit if the corresponding driver software is available for specific combinations of camera and SOM

Please contact PHYTEC for assistance in upgrading a standard Development Kit to an Embedded Imaging Kit.

3.2.3 Connecting the Camera

3.2.3.1 Before Start-Up

Before connecting a camera to the Carrier Board, please read the "Quick Start Instructions" of the respective kit and follow the instructions as described within.

In order to start the scripts on the processor first establish a serial connection between the SOM and the host computer (typically a PC) to which it is connected.

Start the scripts as described in the QuickStart using the recommended terminal software, or any other terminal software.

An Ethernet connection is required to transfer image data to the host-PC. Data is transferred via Ethernet by an FTP connection. We recommend using the FTP software suggested in the Quick Start manual; however, any FTP software should work.

3.2.3.2 Connecting a phyCAM-P camera

Important:

- Power down the system before connecting the camera.
- Be careful not to damage the slide actuator of the connectors.

Open the lock of the 33-pin FFC connector on the camera module. There are two different types of connectors, depending on the camera model. Please determine first, which type of connector is present on your camera:

Shift Lock Connector:
Gently pull the slide actuator out of the connector and slightly lift it upwards as shown in *Figure10*.

Figure10: Inserting the phyCAM-P FFC cable (Shift Lock Connector)

- Next insert the 33-pin FFC cable with the contact side down into the connector until the cable is fully inserted. Ensure that the side of the cable, which is equipped with a stiffener (usually marked by color), is on the same side as the slide of the connector.
- Close the connector by pushing the slide downwards and then gently back into the connector. Make sure the slide is fully inserted on both sides.

Flip Lock Connector:
Gently lift the lock upwards as shown in Figure11.

Figure11: Inserting the phyCAM-P FFC cable (Flip Lock Connector)

- Next insert the 33-pin FFC cable with the contact side down into the connector until the cable is fully inserted. Ensure that the side of the cable, which is equipped with a stiffener (usually

marked by color), is on the same side as the slide of the connector.
- Close the connector by pushing the lock downwards.

Note:
The kit contains a type A FFC cable. Type A indicates that on both ends the contacts are on the same side of the cable. This ensures proper connection of the signal pins. If using other cables, make sure that the contacts are properly oriented. Some cables mirror the contact positions, which might cause damage to the camera and / or Carrier Board.

- Please refer to the description of the Carrier Board in the respective hardware manual to determine the location of the camera connector on the Carrier Board.
  On some Carrier Boards the connector is also labeled "*CAM*" on the PCB silkscreen. The phyCAM-P interface is a 33-pin FFC connector. Depending on the Carrier Board, the connector can be either vertical or horizontal (*Figure12*).
- Perform the steps described above to connect the other end of the camera cable to the Carrier Board.

Note:
Ensure that the camera connector is properly identified. Internal display interfaces might use a connector of the same type.
Make sure not to mix up connectors, as this may damage the camera and / or Carrier Board.

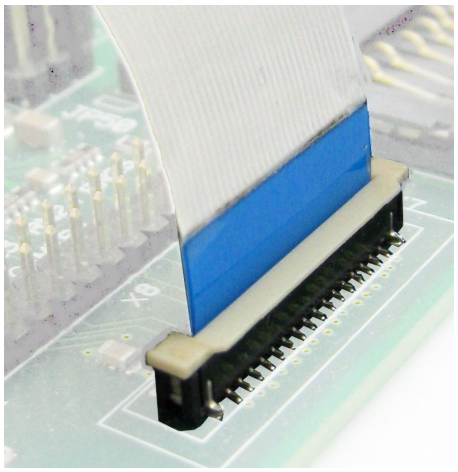


Figure12: Straight-type FFC-connector (phyCAM-P)

Note:
If the Carrier Board is equipped with a vertical FFC connector, the enforced side of the cable has also to be placed on the same side as the slider of the connector (see *Figure12*).

3.2.3.3 Connecting a phyCAM-S camera

Important note:
Switch off the system before connecting the camera.

For the connection of a phyCAM-S camera to a phyCARD Carrier Board, use an adapter cable with an 8-pin Hirose plug on one side and an RJ-45 plug on the other (PHYTEC part #: WK216-0.5).

- Plug the Hirose side into the matching connector of the camera module. The Hirose plug has two guide grooves on the top side. The socket is protected against misinsertion. Assure that the notches of the socket match to the detents of the plug (see *Figure13*).

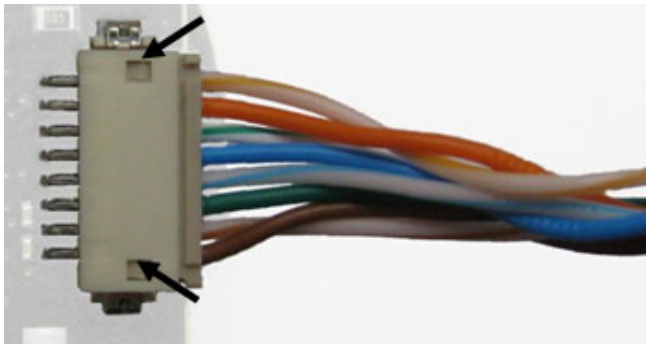


Figure13: phyCAM-S: Hirose type camera connector

- Refer to the hardware manual of the Carrier Board to find the location of the camera connector on the Carrier Board.
  On some Carrier Boards, the connector is also labeled "*CAM*" on the PCB silkscreen. For the phyCAM-S interface, the Carrier Board provides an RJ-45 connector.

Important note:
Most Carrier Boards also provide an RJ-45 socket for the Ethernet interface. Ensure to not mix up the desired RJ-45 camera socket with the Ethernet socket. This may damage the camera and / or the Carrier Board.

- Connect the RJ-45 plug of the camera cable into the RJ-45 socket of the Carrier Board. The slider on the plug is used as reverse polarity protection as well as a lock, thus requiring that the plug is fully inserted and locked.

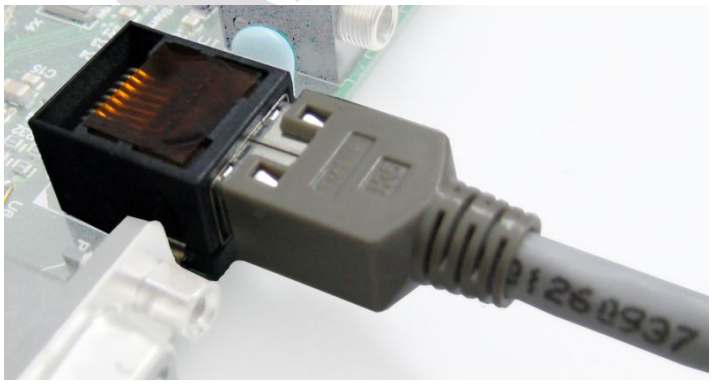


Figure14: RJ-45 Camera connection (phyCAM-S)

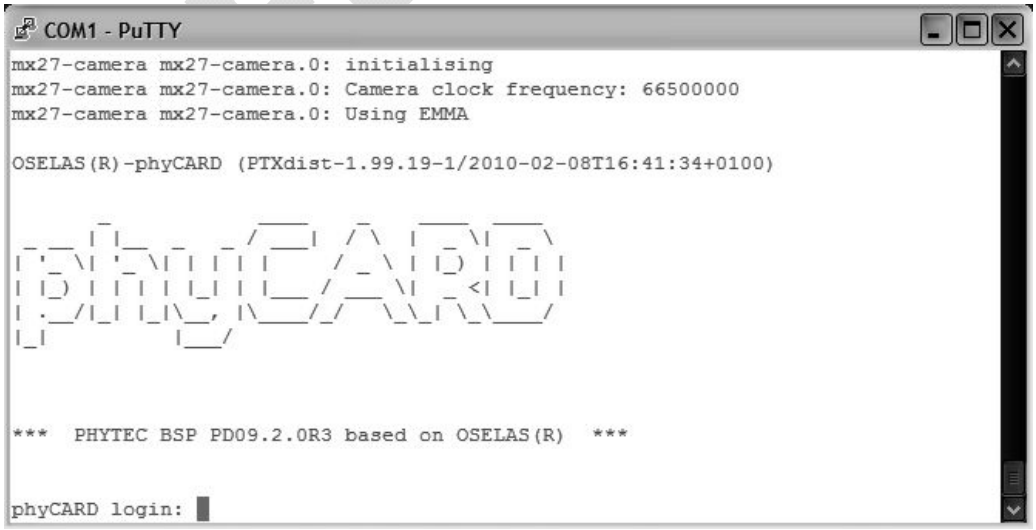
3.2.4 Starting the Demo Application

3.2.4.1 Linux: Starting Script Samples

Before starting the script samples, ensure that the appropriate software driver is installed on the SOM. PHYTEC Embedded Imaging Kits are already configured for the camera that is included in the kit. If using a different camera, the kernel configuration might need adaptation. For example, the camera setting might have to be changed and the corresponding settings in the "*boot-args*". Please read the QuickStart instructions or the "phyCAM – getting started" notes for the applicable Linux BSP.

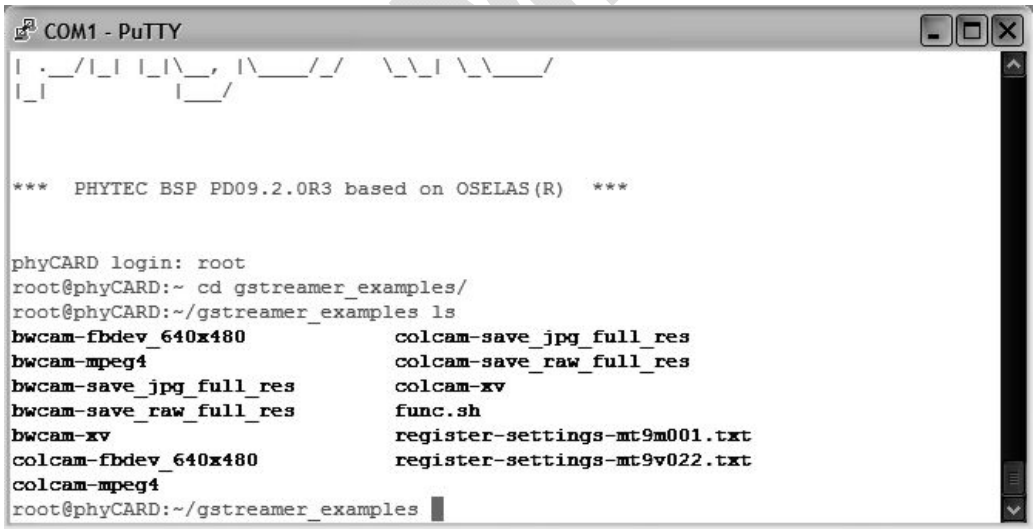
Note:
The example scripts in the root directory are not opimized concerning speed (frame rate), color conversion, resolution etc. For optimized results please use the examples located in the corresponding folders for each camera model.

Start the system once the appropriate driver has been confirmed. This should display boot messages on the terminal window of the serial connection.



Log into the system and list the files and folders present in the home directory using the >*ls*< command.

Next change to the folder with the *GStreamer* samples (cd *xxx* with „*xxx*“ = name of the folder containing the samples). Likewise, list the content of this folder.



Files without extensions are executable script files. The file with extension *.sh* is a shell script, which is used to carry out general settings for the sample scripts.

Files with the extention.*txt* contain additional register settings which can be used together with the *GStreamer-plug-in* “*i2c file*”. For more

details about this plug-in see the *LAN-052 "AppNote_Set_Cam_Register"* application note.

The sample scripts are structured as follows:

- Inclusion of the shell script, such as *`dirname $0`/func.sh*
- Sequence of functions from the shell script, such as *init_dev bw*)
- Start of *GStreamer*, such as *gst-launch* \
- Start of various functions of *GStreamer*, such as *v4l2src !* \

To start a script, simply enter the name of the script on the console of the terminal session, for example:
./colcam-fbdev_640x480 <ENTER>\.

For more information about the free multimedia framework *GStreamer* and included functions, see www.gstreamer.net

PHYTEC's QuickStart Instructions for relevant BSP likewise provide more information about using *GStreamer*.

The table below provides additional information about selected sample scripts.

Sample Script Name	Function	Notes
Showing live images on the system's display		
bwcam-fbdev_640x480	The image of a monochrome (b/w) camera is continuously written into the frame buffer of the microprocessor and is therefore visible on the display connected to the SOM.	The script is configured for a display size of 640x480 pixels. For other display sizes, the image resolution must be adapted.
colcam-fbdev_640x480	The image of a color camera is continuously written into the frame buffer of the microprocessor and is therefore visible on the display connected to the SOM.	The script is configured for a display size of 640x480 pixels. For other display sizes, the image resolution must be adapted.
all other *fbdev* scripts	Image data is written to the frame buffer of the SOM.	Samples with different resolution settings and ROI functions.
Storing an image. Note that images stored on the SOM can be transferred to a host computer using an FTP connection. This is useful for testing.		

bwcam-save_raw_full_res	Stores the image data of a monochrome (b/w) camera as the file “bw_image.raw”.	The data is written in raw format without any overhead or header data.
colcam-save_raw_full_res	Stores the image data of a color camera as the file “col_image.raw”.	Format without any overhead or header data.
bwcam-save_jpg_full_res	Transforms the image data of a monochrome camera into JPEG format and stores the image as the file “bw_image.jpg”.	Image data is stored as a JPG-image.
colcam-save_jpg_full_res	Transforms the image data of a color camera into JPEG format and stores the image as the file “col_image.jpg”.	Image data is stored as a JPG-image.
Streaming live images via Ethernet		
bwcam_xv	Streams uncompressed, monochrome (b/w) image data to a X-server host.	Needs Ethernet connection and appropriate receiver (host with X-server). Refer to OSELAS QuickStart guide. Before the script is called, the target display has to be initialized (export DISPLAY=<IP>:0“)
colcam_xv	Streams uncompressed, color image data to a X-Server host.	Needs Ethernet connection and appropriate receiver (host with X-server). Refer to OSELAS QuickStart guide. Before the script is called, the target display has to be initialized (export DISPLAY=<IP>:0“)
bwcam_mpeg4 *Notes:* *Not available at all kit variants.* *If the CPU supports more stream formats, other examples can be found in the corresponding folder.*	Streams MPEG4-compressed, monochrome (b/w) image data to a X-Server host.	Needs Ethernet connection and appropriate receiver (host with GStreamer). Please note that adaptations to the scripts are necessary prior to usage, such as setting the IP-address. **Important note:** This script works only on selected SOMs. It is recommended for experienced Linux users only.

colcam_mpeg4 *Notes:* *Not available at all kit variants.* *If the CPU supports more stream formats, other examples can be found in the corresponding folder.*	Streams MPEG4-compressed, color image data to a X-Server host.	Needs Ethernet connection and appropriate receiver (host with GStreamer). Please note that adaptations to the scripts are necessary prior to use, such as setting IP-address. **Important note:** This script works only on selected SOMs. It is recommended for experienced Linux users only.

Note:
PHYTEC continuously improves the scripts included in kits. Depending on the kernel version, SOM and camera module, these samples might vary.

Scripts written for a certain camera module or camera sensor are located in a separate folder. The folder names refer to the camera sensor's name. Please not that some scripts might be only available for certain hardware platforms, such as phyCARD and/or phyCORE only.

3.2.4.2 Starting the Windows Embedded CE Demo Application

- Start the SOM and Carrier Board system and watch the kit display. After the boot process is completed, the Windows desktop appears:

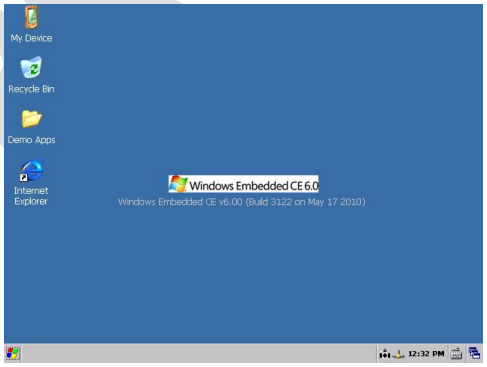


Figure15: Windows Embedded CE Desktop

- Check if the camera configuration of the system matches with the camera connected to the SOM/Carrier Board combination. To do this, start the *CamSel* – application in the path: *Start/Settings/Control Panel/SelCamera*.

Figure16: SelCamera (icon)

- In case the camera connected to the SOM/Carrier Board combination is not listed as *Current*, click on the corresponding button to change to the camera of choice.

Figure17: SelCamera (application)

- A popup-window will appear to indicate that changes made to the registry have to be saved before these changes are made active.

Figure18: SelCamera (registry hint)

- To save the registry and make the changes persistent, start the *SaveReg.exe* Application from the path: *My Device/Windows/…*

Figure19: SaveReg (icon)

Important note:
- Each change of the camera type requires change and save of the registry settings.
- NOTE: **Changes to the registry only come into effect after the system has been restarted.**

Restart the system to activate the new camera setting.

- Now start the demo application *CameraApp.exe* which is in the Windows – folder of the embedded system (*My Device/Windows/…*).

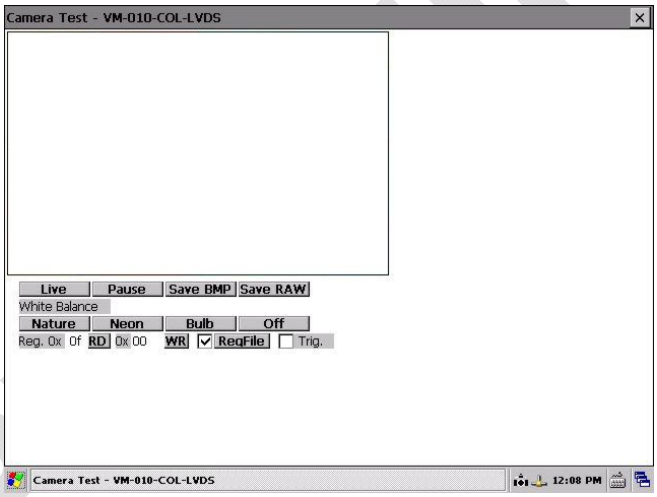


Figure20: Windows Demo Application

- The first time the application is opened, or in case the register settings file ("*register-settings-xxx.txt*" with *xxx* = camera type) has been lost, this configuration file will be generated and stored in the folder */NandFlash/…* .
  The following message box will confirm this operation (message text might be in German):

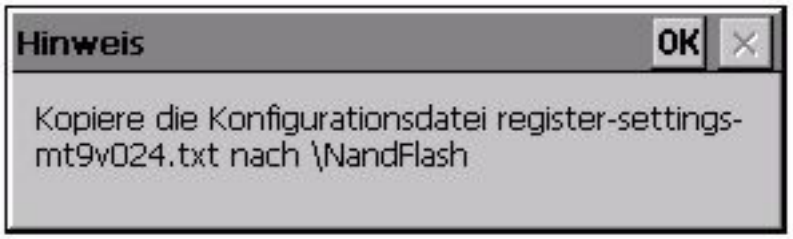


Figure21: Windows Demo Application (info box)

- When selecting the <live> button of the demo software, a live image will be requested from the camera. If a camera is connected, an image should display as shown in *Figure22*.

Figure22: Windows Embedded CE – demo application showing live image of a color camera

The demo application features the following basic functions:

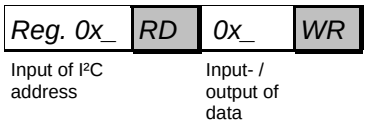
Button	Function	Remarks
Basic Functions		
	Image data from the camera is	The image size adapts to the

Live	continuously read and written to the image window (“live image”)...	resolution of the display contained in the development kit. If necessary, a color conversion is performed, such as if color cameras with Bayer pattern output are used
Pause	Pauses the live image function. Display shows a still image.	Press Pause again to return to live image mode.
Save BMP	Captures a still image, converts the image data into bitmap (BMP) format and saves it as ”capture.bmp”.	The image is captured at maximum resolution. The file is stored in the “My Device” folder.
Save RAW	Captures a still image and saves it as raw pixel format as ”capture.raw“, such as in Bayer pattern format for certain color cameras	The image is captured at maximum resolution. The file is stored in the “My Device” folder.
*Reg. 0x_* *RD* *0x_* *WR*	Read (RD) or write (WR) internal registers of the camera sensor. See example below. Note that some registers are write-protected.	Values are entered / shown in hexadecimal format. **Note:** Changing camera registers might set the system into an undefined state / block camera access.
extended Add-On functions:depending on camera and software version		
White Balance: *Nature* *Neon* *Bulb* *OFF*	Adapts the white balance of a color image, if image is converted from Bayer format (RGGB) to RGB. RGB channels are weighted by a correction factor.	Example of factors for VM-007 / VM-010: Nature ⇨ R = 1.3 / G = 1 / B = 0.8 Neon ⇨ R = 1 / G = 1 / B = 1.9 Bulb ⇨ R = 0.6 / G = 1 / B = 2.1 OFF ⇨ R = 1 / G = 1 / B = 1
☑ *Regfile*	☑ Activates/deactivates the use of a register set file to initialize the camera at the start of the demo application. Tap on *Regfile* to select a register set file.	The selected register set file is loaded upon startup of the demo application only if the feature is activated. Use *”savereg“* to save the setting changes even after a new startup of the Windows system.
☑ *Trigger*	Activates/deactivates the single shot mode of the camera.	**Note:** An image is only taken if an external trigger pulse occurs. Note: ensure proper jumper settings of the camera module PCB.

Note:

- **Reading and writing data from/to sensor registers**
  This allows direct adaptation of features and settings of the

camera sensor to the needs of a specific end application. Data is entered by the register mask of the application:



For reading a register value, enter the register address into the field *Reg* (hexadecimal format) and select the *RD* button. The data value read from the register is shown in the field that appears after *RD*.

To change a register content, enter the I²C-address of the register into the *Reg* address field, enter the value to be written into the data field behind *RD*, and select the *WR* button.

Please note that not all registers grant write access. Changing register contents might lead to undefined behavior of the camera.

- **Using a register set file**
  Using a register set file is an easy way to customize register content of the camera without entering each value manually. A text file (.txt) is used to define the complete register set. Content can be modified according to end user needs.

  First, make a copy of the configuration file "*register-settings-xxx.txt*"(*xxx* = sensor type).

  Next, edit a copy of the file and save the changes. Tap on the Regfile button and specify the register set file to use. Activate the feature by tapping on the checkbox ☑ in front of the *Regfile* button.

  Note:
  - If the feature is not activated (box ☑ not checked), only the default values that are stored *in the camera driver* are loaded.
  - Settings are **not** changed immediately but only upon next start of the demo application.

- For more information about defining register sets please see the application note *LAN-052-e_"AppNote_Set_Cam_Register"*.
- Settings are only persistent for this Windows session. They are lost on the next start of the system. Use *SaveReg.exe* (from *My Device/Windows/…)* to permanently store the settings of this feature.

3.2.5 Troubleshooting

This section illustrates tips for troubleshooting in the event of problems with startup.

3.2.5.1 Display Test

Linux:
Enter *fbtest <ENTER>* on the console. The display should show several test patterns for metrics and color schemes.

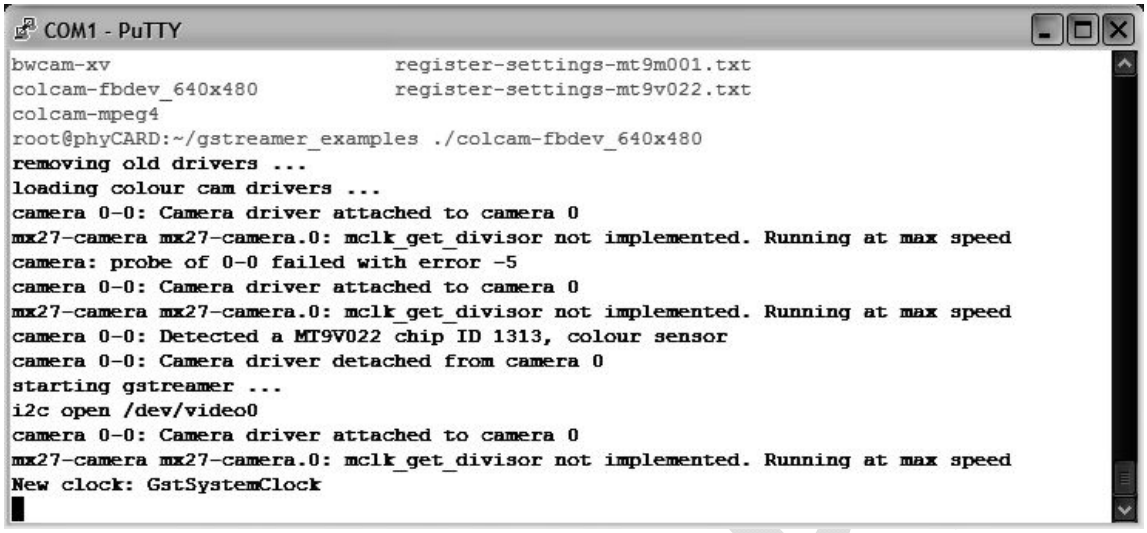
Windows Embedded CE:
Verify if the colors on the Windows desktop are displayed properly.

Potential problem:
No image is shown on the display of the kit hardware:

Troubleshooting:
- Check the connection of the display cable.
- Check if the backlight is operating (cable connection etc.).

3.2.5.2 Camera Live Image Test

Linux:
Enter the name of a script file matching the deployed camera (color / monochrome) as well as display resolution on the console.
Sample:
./colcam-fbdev_640x480 <ENTER>

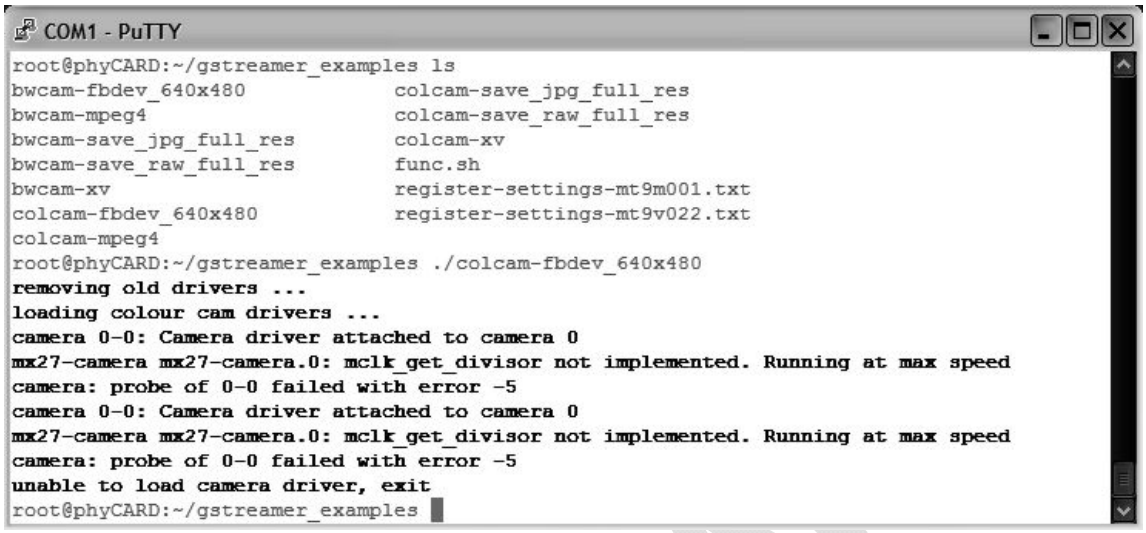


The script will automatically load the appropriate drive for the camera or checks which driver has been loaded. If a camera sensor connected to the system is found, a message similar to the following will be displayed on the console, and a live image will be shown on the display:
camera 0-0: Detected a MT9V022 chip ID 1313, color sensor

Windows Embedded CE:
Use the demo application to test the camera. In order to test the camera in live-mode, tap the <*Live*> button of the application.

Potential problem:
No camera is found.

Linux:



Windows Embedded CE:
No image is shown in the window.

Troubleshooting:

- Check the connection of the camera cable.
- *Linux*: check if the camera is supported by the kernel version.
- *Linux:* check if new versions of the *GStreamer* samples are available.
- *Linux:* try to load the camera driver manually by using the *modprobe* command.
- *Windows Embedded CE:* check if the correct camera driver is selected by using *SelCam*.

Potential problem:
The live image is shown with noticeable delay as well as low framerate.

Troubleshooting:
This is not a problem. Due to several reasons, a live image might not be shown at maximum framerate due to the following factors:

- Very high image data volume caused by a high image resolution, color format, or other reason
- Algorithms used for image processing consume lots of CPU power.

- Color space conversion has to be carried out by the microprocessor, such as Bayer Pattern to RGB.
- Microprocessors feature different calculation speeds and different multimedia units. Multimedia accelerators might not be supported by the demo application.
- *Linux:* Note that *GStreamer* is a modular framework. Therefore it is not always optimized for high speed applications.

The user should reduce the amount of image data and use speed-optimized algorithms adapted for specific tasks and use cases.

3.3 How to change the settings of the camera sensors

The camera sensors offer numerous options to control and fine-tune the image acquisition.
In general these settings are made by changing the values of the camera sensor's registers. The register contents are accessed by the I²C interface of the sensor.
The camera sensor driver already controls many register settings automatically when the camera device is opened or certain camera functions are invoked.
However, some special settings can not be accessed via the V4L2 driver (like, for examply, the settings for HDR mode that is provided by some cameras).
In this case the application software developer can use direct register access via the I²C driver to read, write and modify the settings of the camera's registers

3.3.1 Basics

The phyCAM digital camera modules are supported by the BSPs shipped with the Phytec microcontroller boards (SOMs).
The name of the corresponding drivers reflect the sensor chip of the camera module.

Examples:

- VM-006 series : Aptina mt9m001

- VM-007 series : Aptina mt9v022
- VM-009 series : Aptina mt9m131
- VM-010 series : Aptina mt9v024
- VM-011 series : Aptina mt9p031

Note that the camera modules supported for a given BSP might vary for different SOMs. Phytec is constantly improving the support for the camera modules with new BSP versions.
Please check if a certain camera module is supported by the BSP version before starting with your develoment.

Linux:
With Linux the cameras are accessed via the *Video4Linux 2* – interface (V4L2).
This allows access to image data directly from application software.Also multimedia frameworks like *GStreamer* can access the camera via the V4L2 interface.
Note that V4L2 implements many functions for different device types. Not all functions are available for the phyCAM camera modules. It's recommended to determine the supported functions by using the *Capability Querying*. This procedure and a detailed description of the V4L2 functions can be found in the *Video for Linux Two API Specification*.

Windows CE / Windows Embedded Compact:
The camera drivers for Windows Embedded are compatible to *DirectShow*.
Please see the demo application shipped with the development kit as a reference of how to access the camera data from your own application. More informations can be found in the brief description of the corresponding drivers.
Die digitalen phyCAM-Module werden durch die passenden Kameratreiber im PHYTEC BSP des Embedded-Controllerboards unterstützt.

3.3.2 Access to the camera registers

Important Note

The correct setting of some camera registers are fundamental for the function of the camera and an undisturbed image acquisition.

Changing the contents of these registers will result in image desturbances or an unstable system behavior.
Because of this Linux allows a manual modification of the registers **in debug mode only**.

Before changing any camera settings please verify carefully that the modifications will not harm the camera function nor affect the stability of the system.

Some registers are controlled by the V4L2 camera driver.
This means that changing these registers might affect the behavior of the driver.
On the other hand, some settings might be overwritten by the V4L2 driver, for examples when certain driver functions are executed. Thus these settings might not take any effect when followed by a driver call.

3.3.2.1 General Register Access (Linux)

To access the camera register with Linux the following V4L2 APIs can be used:

- *VIDIOC_DBG_G_REGISTER*
- *VIDIOC_DBG_S_REGISTER*

Important Note:
These functions can oly be used if the driver is compiled in **debug mode** (*CONFIG_VIDEO_ADV_DEBUG*)!

The camera drivers shipped with the Phytec distribution are already compiled in debug mode.

The functions for register access can be used in custom application software.
Before the integration of register settings into the application software, it might be a good idea to test the effects with simple tools. For this purpose Phytec ships a plugin for the popular *GStreamer* framework with the Embedded Imaging Kits.
The *GStreamer* framework can be configured by simple script writing. The example scripts that come with the kits use the *GStreamer* for

demos like transmission and viewing image streams or saving single shots and live streams to memory in various formats. See the phyCAM manual (L-748), section 3 for more information about the example scripts.

3.3.2.2 General Register Access (Windows)

For Windows Embedded standard I²C routines can be used to access the camera registers.
The Phytec BSP contains already these functions and these functions are also called by the camera driver.

The functions for register access can be used in custom application software.
Before the integration of register settings into the application software, it might be a good idea to test the effects with simple tools. Phytec ships a demo application with the Embedded Imaging Kit which allows to alter register contents and to watch the changes in the live image.

3.3.3 Register Definition File

For adapting the camera characteristics to a certain use case it is helpful to alter several registers at once. For this Phytec provides a tool that loads the register map from a text file into the camera registers.
Also, predefined register files (*use cases*) are provided for many cameras. The register files can be edited by using a standard text editor.

3.3.3.1 Register File Syntax

For each camera module an example for a register definition file comes with the development kits.
In the kits the following name convention is used, however, any file name can be used for custom register definition files:

- „register-settings-mt9v022.txt“ (VM-007)
- „register-settings-mt9m001.txt“ (VM-006)
- „register-settings-mt9m131.txt“ (VM-009)

The content of a register definition file must be in accordance with the following syntax:

chip-address, register-address, value, [mode]

chip-address =	I²C device address of the camera sensor. Format: 8 bit hex Examples: MT9V022 = 0x48 / MT9M001 = 0x5D
register-address =	Register address of the register that is to be written. Format: 8 bit hex
value =	value to be written to the register specified by *register-address* Format: Either 16 bit hex (leading 0x...) or decimal
mode =	optional, allows a logical operation of *value* and the current register content. Parameters: a (AND, bitwise AND of current content and *value*) o (OR, bitwise AND of current content and *value*), x (XOR, bitwise XOR of current content and *value*)

Comments can be included by a leading hash (#).

Note:
This is a simple way to switch a certain modification on or off. See example below.

The example definition files shipped with the BSPs already inculde many options with most of them set inactive by a leading #.
For testing a specific setting just remove the # at the beginning of the line.

Example:
For the MT9V022 sensor (VM-007) the AGC level (automatic gain control) is to be set to gain factor x2.

To acheive this, the # at the beginning of the corresponding line was removed (line printed bold in the example below):

```
---------------------------
#  set MT9V022 AGC
#  ===============
#  set AGC automatic
#0x48,0xAF,0x0002,o # automatic = on

#  set AGC manual
0x48,0xAF,0xFFFD,a  # automatic = off
#0x48,0x35,0x0010   # set gain = 1.00
#0x48,0x35,0x0014   # set gain = 1.25
#0x48,0x35,0x0018   # set gain = 1.50
#0x48,0x35,0x001C   # set gain = 1.75
0x48,0x35,0x0020    # set gain = 2.00
#0x48,0x35,0x0024   # set gain = 2.25
#0x48,0x35,0x0028   # set gain = 2.50
#0x48,0x35,0x002C   # set gain = 2.75
#0x48,0x35,0x0030   # set gain = 3.00
…
---------------------------
```

After loading the register settings into the camera the image is captured with a fixed gain setting of 2. The predefined register definition files include more optional settings for the individual camera modules.

For more informations about the register settings of a camera sensor see the datasheet of the sensor. Datasheets for the sensor chip can be downloaded from the sensor manufacturer's website (for example for MT9M001, Mt9V022 see www.onsemi.com).

We recommend using a FTP connection between the developent computer and the embedded system for transferring register definition files between PC and the target system. This allows a comfortable editing of the file.

The predefined example files for the camera sensors are located:

- for **Linux** in the same directory as the example scripts for the GStreamer …`/gstreamer_examples/`…

- for **Windows** in the folder …/NandFlash/.. .
  In case the register definition file in this location is deleted or renamed the demo software will create a default file.

Note

If a register definition includes more than one definition for a dedicated register the definitions are written in the same order as they are listed in the file.
This means that the value of the last definition is in effect after the register upload has finished. However, all other write commands have been executed before (and might have had affected the sensor's behavior).
Take care that a desired setting is not overwritten by a later definition of the file, especially if you are using the comment (#) method.

In connection with the logical operands (AND, OR, XOR) consecutive write commands can be helpful to modify only certain parts of a register (bit masking).

Example:
Setting the lower byte of a register to 0x35 without altering the upper byte:

```
chip-address, register-address, 0xFF00,a # clear lower
byte
chip-address, register-address, 0x0035,o # write 0x35
to low-byte
```

3.3.4 How to use the Register Definition File (Linux)

3.3.4.1 GStreamer function

The script examples shipped by Phytec show how the *GStreamer*-examples can be extended with regsister file upload.

In the first step, the desired camera configuration is set by editing the register definition file. This can be done by adding / removing the comment signs (#) from certain lines or adding new register definitions.
In the second step this file is uploaded by a GStreamer command added to the pipeline.

3.3.4.2 Requirements

- Make sure that the camera driver used has been compiled in debug mode (see section **Fehler! Verweisquelle konnte nicht gefunden werden.**). The camera drives shipped with the Phytec BSPs are already compiled in debug mode.

- *GStreamer* - plug-in for register upload (part of the Phytec distribution)..

3.3.4.3 Example of applying a register definition (Linux)

This example shows how to use a register definition file with the *GStreamer* framework.
For this demonstration we use the *bwcam-save_jpg_full_res* script for the VM-007-BW (mt9v022) camera module.
This script captures a single shot image from the VM-007-BW camera and saves it to a JPEG-file.
The image sensor of the VM-007-BW module (Aptina MT9V022 sensor) is operated with its default settings in automatic mode. Thise means AGC/AEC and atuomatic BLC are enabled.

The script looks like this:

```
---------------------------
#!/bin/sh

. `dirname $0`/func.sh

init_dev bw
[ $? -ne 0 ] && exit 1

guess_res
```

```
echo "starting gstreamer ..."
gst-launch \
     V4L2src num-buffers=1 ! \
     video/x-raw-gray$FRAME_SIZE ! \
     ffmpegcolorspace ! \
     video/x-raw-yuv$FRAME_SIZE ! \
     jpegenc ! \
     filesink location=bw_image.jpg
---------------------------
```

To upload register settings to the camera sensor, we have to add the plug-in ***i2c*** to this script. When processed by the GStreamer pipeline, this script uploads the register settings from a text file to the specified camera (see syntax in section **Fehler! Verweisquelle konnte nicht gefunden werden.**).
The plug-in syntax needs the following parameters:

```
i2c file=[name of register definition file]
show=0
```

It's important to place the plug-in at the right position in the script so that the settings are not overwritten by another process.
A good place for our example is between the initialization and the image capture call:

```
---------------------------
     …
     V4L2src num-buffers=1 ! \
     i2c file=register-settings-mt9v022.txt show=0 ! \
     video/x-raw-gray$FRAME_SIZE ! \
     …
-------------------------
```

The register definition file (here: *register-settings-mt9v022.txt*) is loacted in the working directory.
Setting of the parameter *show=1* echos the register access also on the serial interface (console output).

Type `gst-inspect i2c` to list more parameter options for the plug-in.

Note:
If there is more than one camera present in a system, the parameter `addr=[i2c hex_address of the device]` allows to use

the same definition file for more cameras of the same type but different I²C addresses.
Adding the `addr-` parameter will ignore the I²C addresses defined in the file and replace them with the address specified.
Example for video-device_0 at address 0x48 and video-device_1 at addresse0x4C:

```
 i2c addr=0x48 file=register-settings-mt9v022.txt
show=0  dev=/dev/video0 ! \
 i2c addr=0x4c file=register-settings-mt9v022.txt
show=0  dev=/dev/video1 ! \
```

3.3.5 Applying the Register Definition File (Windows)

3.3.5.1 Windows Embedded Demo Software

The Demo Software for Windows CE / Embedded shipped with the Embedded Imaging Kit allows to upload register definition files to the camera.

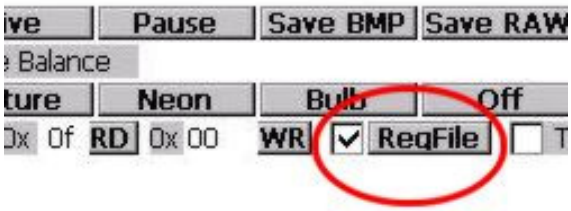
3.3.5.2 Requirements

A register definition file has to be present on the sytem.
For example in the folder `.../NandFlash/...` (part of the Phytec distribution).

3.3.5.3 Example of uploading a register definition (Windows)

Start the demo application *CameraApp.exe* which is located in the Windows-Folder (*My Device/Windows/…*) on the embedded System.

Cick on the *RegFile* – button of the application to select a register definition file.
Activate the register upload by selecting the RegFile function checkbox: ☑



To make this settings permanent, call the *savereg* function after closing the demo application. By this, the contents of the register file will be uploaded to the camera automatically every time the demo application is started.
In case the register definition file in this location `.../NandFlash/...` is deleted or renamed the demo software will create a default file.

4 Technical Specification phyCAM-P Camera modules

This section lists the specification of each camera module, including: features, special functions and configuration options.
Camera modules are listed by PHYTEC part numbers.

4.1 VM-006-BW - phyCAM-P camera module

1.3 Megapixels / monochrome

4.1.1 Specifications

Features

- 1.3 Megapixel image sensor, monochrome
- phyCAM-P – parallel interface
- Frame rate up to 30 fps
- Rolling shutter
- High dynamic range
- External trigger and strobe
- Multiplexer for on-the-fly 8- / 10-bit format selection (optional)
- 3x I/Os
- Secondary connector with trigger, strobe and I/O (optional)

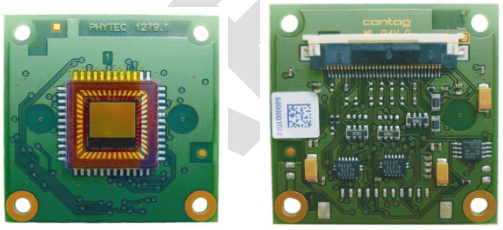


Figure23: phyCAM-P (VM-006-BW) (front / rear view)

Parameters

	VM-006-BW	VM-006-BW-MUX
Sensor		
Resolution	1.3 Mpixels	1.3 Mpixels
Pixels (H x V)	1280 x 1024	1280 x 1024
Sensor Size	1/2" 6.66 x 5.32 mm	1/2" 6.66 x 5.32 mm
Pixel Size	5.2 x 5.2 µm	5.2 x 5.2 µm
Color / Monochrome	monochrome	monochrome
Technology	CMOS	CMOS
Image Sensor	Aptina MT9M001	Aptina MT9M001
Scan System	progressive	progressive
Shutter Type	rolling	rolling
Frame rate (fps) full resolution	up to 30 fps	up to 30 fps
Video Resolution	n/a	n/a
Responsivity	1.2 V/lux-sec	1.2 V/lux-sec
max. Dynamic Range	68.2 dB	68.2 dB
High Dynamic Range	-	-
Exposure Time	programmable	programmable
Gain	x1...x15	x1...x15
AEC	-	-
AGC	-	-
Gamma Correction	-	-
White Balance/AWB	n/a	n/a
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	yes	yes
Skipping	2 / 4 / 8	2 / 4 / 8
Mirror	programmable	programmable
Image Processor	-	-
LED Lightning	-	-
Special Functions	see section 4.1.4	see section 4.1.4

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-P	phyCAM-P
Data Format	8-/ 10-Bit parallel	8-/ 10-Bit parallel
Interface-Mode	Y8 / Y10	Y8 / Y10
Dataline-Shifting	-	yes
Camera Config. Bus	I²C	I²C
Supply Voltage	3.3 V	3.3 V
Power Consumption	363 mW	363 mW
Pwr. Consumpt. Standby	294 µW	294 µW

Mechanical Parameters		
Lens Connector	none / M12 / C-CS	none / M12 / C-CS
Lens	-	-
Housing	-	-
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	-	-
Weight (PCB)	7 g	7 g
Operating Temperature	0...70°C	0...70°C

Connectors		
Data and Power	FFC 33-pin	FFC 33-pin
Trigger / Sync.	FFC + Molex 11-pin	FFC + Molex 11-pin
Iris	-	-
Special functions	-	-

n/a: not applicable. All parameters are subject to change.

Table 9: VM-006-BW (phyCAM-P) Parameters

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operating Current	I_{CAM}	-	125	-	mA
Input high voltage	V_{IH}	V_{CAM} -0.3	-	V_{CAM} +0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Output high voltage	V_{OH}	V_{CAM} -0.3	-	-	V
Output low voltage	V_{OL}	-	-	0.2	V
Voltage Set Resistor	R_{31}	-	0	2	Ω
Operating Temperature	T_{OP}	0	-	70	°C
Storage Temperature	T_{STG}	-40	-	125	°C

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	1	-	48	MHz
Clock Duty Cycle	$dutycyle_{MCLK}$	45	50	55	%
MCLCK to PCLK delay	t_{CP}	-	10	-	ns
PCLK to data valid	t_{PD}	-	-	1	ns
PCLK to Sync high	t_{PVH}	-	-	7	ns
PCLK to Sync low	t_{PVL}	-	-	13	ns
I²C Frequency	f_{I2C}	-	100	-	kHz

Data Formats

Monochrome:

- Y8 : 8-bit grey scale
- Y10: 10-bit grey scale

Notes

- Any other desired, lower color / grey scale resolution can be configured by using a reduced subset of the data lines. To configure this, connect only the upper data lines (MSB) to the microprocessor interface. Some microprocessors also enable dynamic configuration of the camera interface input.
- The –MUX variant allows dynamic (on-the-fly) switching of the data output format of the camera between Y8 and Y10 (see section 4.1.4.1).

Spectral Characteristics

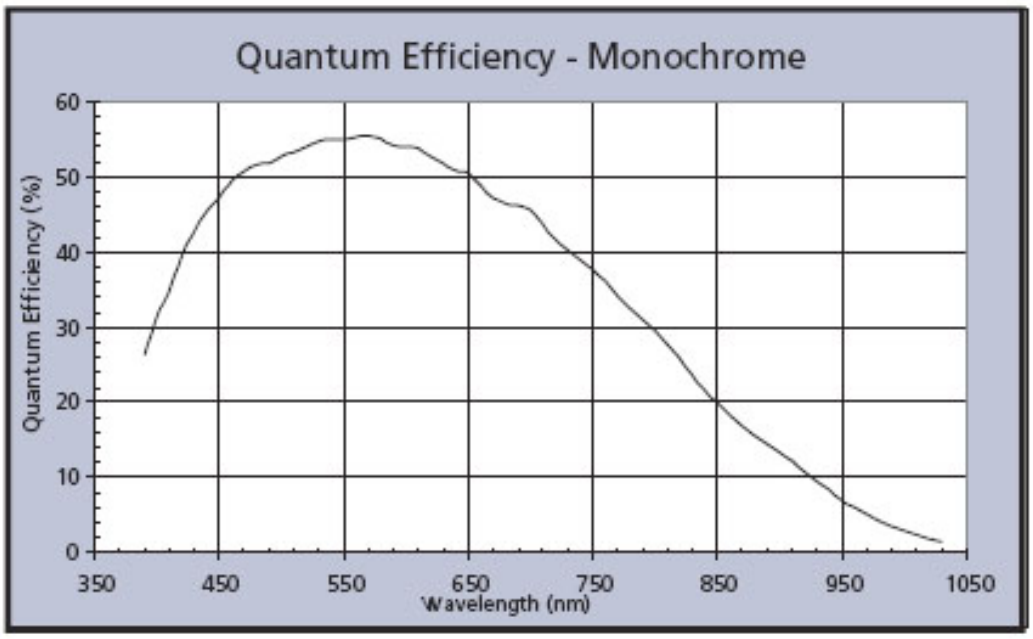


Figure24: VM-006-BW Spectral Characteristics

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

4.1.2 I²C Addresses

Device	I²C-Address	Configuration	Variant
Camera Sensor	0xBA		all
Bus-Multiplexer / I/O	0x82		-MUX

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with 7-bit Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

4.1.3 Feature Pins

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	external Trigger	I	R105=0R
CAM_CTRL2	30	GND	-	hardwired to ground
CAM_RST	3	/Camera Reset	I	active low
CAM_OE	32	**n/a (open)**	**-**	**R103=NOMT, R104=0R**
		/Data Output Enable	I	active low R103=0R, R104=NOMT

Note:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

4.1.4 Special Features

4.1.4.1 Dataline-Shifting

This function is available with the –MUX option only.

Camera interfaces of various microprocessors use different data bus widths. For example, a processor might support an 8-bit or 10-bit camera interface. Some processors allow software configuration of the bus width according to the interface of a camera module and its underlying camera sensor.

In addition a particular application might define the width of the data bus, since the width of the camera interface defines the color depth. A

wider interface allows a more precise representation of the brightness or color information of a pixel.

Example: If an application demands a high color depth, such as 10-bit, all 10 data lines of the camera are connected to the microprocessor interface. If a standard resolution of 8-bit is sufficient, the lower 2 data lines of the camera are left unconnected. Only the upper 8 lines are wired to the microprocessor interface, connecting D2 of the camera to D0 of the microprocessor.

However, some applications might require both options. Therefore it is advantageous to switch between 8-bit and 10-bit mode during operation.

Example:
For a precise measurement application, 10-bit color depth is needed. On the other hand, the application might also feature a viewfinder option. For this, 8-bit mode is more convenient because 8-bit mode does not need any data format conversion to send the data to the display.

Some microprocessors already feature a dynamic configuration of the interface format. For other processors that do not feature this – such as the Marvell PXA270/PXA320 - the –MUX feature allows dynamic configuration on the camera module.

With the –MUX option, an additional multiplexer on the camera module shifts the data lines by two (see *Figure25*). Thus, D[9..2] of the sensor are routed to D[7..0] of the interface. The multiplexer is controlled by I²C commands.

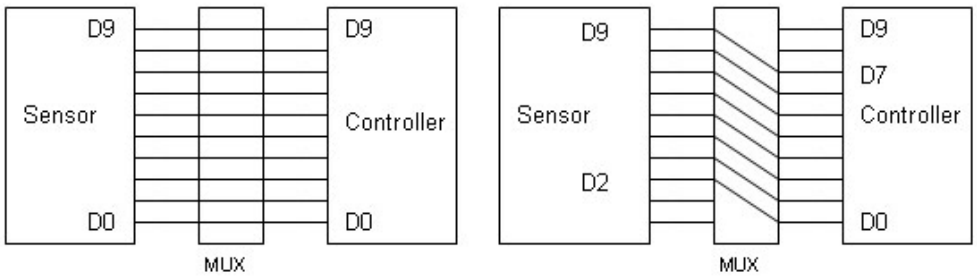


Figure25: Dataline-Shifting

Configuration of the data lines is done by data bit 0 of the I²C parallel port interface on I²C address 0x82, register address 0x01:

Data Bit	State	Function	Notes
0	0	10-bit image data	dataline-shifting not active (default)
0	1	8-bit image data	dataline-shifting active

Notes:

- The data direction of bit 0 must be set to output prior to using this function.
- Do not alter other bits of the registers, since they are used for the I/O port feature.
- Refer to the PCA9536 I²C port device datasheet for more information.

Registers:

Dataline-Shifting								
Device 0x82 – Register 0x00								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	IO_3	IO_2	IO_1	Dataline Shift

Dataline-Shifting – Data-Direction Register								
Device 0x82 – Register 0x03								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	DIR IO_3	DIR IO_2	DIR IO_1	0

Assignment of data lines:

Image Data Out	Sensor Interface	
	Shifting not active	Shifting active
CAM_DD0	D0	D2
CAM_DD1	D1	D3
CAM_DD2	D2	D4
CAM_DD3	D3	D5
CAM_DD4	D4	D6
CAM_DD5	D5	D7
CAM_DD6	D6	D8
CAM_DD7	D7	D9
CAM_DD8	D8	D8
CAM_DD9	D9	D9

4.1.4.2 Trigger

Using the trigger input allows precise control of the point in time an image is captured by an electrical signal. When the camera is in *snapshot-mode*, a high-level at the trigger input starts a capture process. When using the *Continuous-Video Mode* (live image mode, default), the trigger input should be held at low-level (GND) or left open. For details about the trigger mode, please refer to the sensor datasheet.

The trigger input is available at the pin *CAM_CTRL1* of the phyCAM-P connector (R105 has to be populated). Furthermore, the trigger input is available at pin 3 of the expansion connector.

4.1.4.3 Strobe

A high pulse at the strobe output indicates that the image array of the sensor has been reset. It indicates that the capture of an image has been completed. For details about the strobe signal, please refer to the applicable camera sensor datasheet. The strobe signal is available on pin 4 of the extension connector.

4.1.4.4 Reset

If there is a low-level reset input to GND low-level, this initiates a reset of the camera sensor. All registers are set to their default values. The reset input should be connected to the /RESET output of the SOM. The reset signal must be held on high-level during operation of

the camera module.

Note: The reset input does not reset either the I²C I/O device or the multiplexer (-MUX option).

4.1.4.5 Output-Enable

The output-enable input allows control of the signal lines CAM_DD[0...9], CAM_LV, CAM_FV, CAM_PCLK and STROBE. Applying a high-level to this input will tristate these outputs. For normal operation, output enable must be at low-level (GND).
The output enable feature is not available with the –MUX version.

Note that R103 / R104 must be properly set to enable this function. In default configuration, this feature is not available. Outputs are always active.

4.1.4.6 I/O-Port

The –MUX variant of the camera module features three I/O signals. These signal lines can be used as either inputs or outputs, depending on the configuration of the I²C port device. The I/O lines can be configured and read/written by the port device at I²C address 0x82:

I/O-Port – Output Register								
Device 0x82 – Register 0x00								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	IO_3	IO_2	IO_1	Dataline Shift

I/O-Port – Input Register								
Device 0x82 – Register 0x01								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	1	1	1	1	IO_3	IO_2	IO_1	Dataline Shift

Dataline-Shifting – Data-Direction Register								
Device 0x82 – Register 0x03								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	DIR IO_3	DIR IO_2	DIR IO_1	0

Each line can be configured individually to act as input or output in the *Data-Direction* register. Setting the corresponding bit *DIR_IO_x* = 1 configures the line as input. This is the default setting. Clearing the bit (*DIR_IO_x* = 0) configures the line as output. The *input register* enables reading of the corresponding signal level via the output register. Please note that bit 0 is reserved for the *dataline-shifting* function and must not be altered.

For more information about programming the interface and the electrical parameters of the I/O lines please refer to the PCA9536 I/O device datasheet.

4.1.4.7 Expansion Connector

An 11-pin, 1.25mm expansion connector can optionally populate the camera module. This connector is a Molex PicoBlade (Molex part # 53261, right angle; Molex part # 53398, vertical).

Extension Connector VM-006 (optional)			
Pin	**Signal**	**Dir**	**Function**
1	Vcam	-	Supply voltage camera
2	GND	-	GND
3	CAM_TRG	IN	Trigger input (optional also at CAM_CTRL1)
4	CAM_STROBE	OUT	Strobe output
5	CAM_CTRL1	-	CAM_CTRL1 of CAM-P connector
6	CAM_SDA	I/O	SDA I²C bus data line of phyCAM-P connector
7	CAM_SCL	O	SCL I²C bus clock line of phyCAM-P connector
8	IO_1	I/O	user I/O pin (–MUX variant only)
9	IO_2	I/O	user I/O pin (–MUX variant only)
10	IO_3	I/O	user I/O pin (–MUX variant only)
11	GND	-	GND

Signal direction denoted with respect to camera module.

Table 10: VM-006 Extension Connector

4.1.5 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

4.2 VM-007 - phyCAM-P camera module

Wide-VGA / monochrome, color

Note:
This part is not available for new designs.
Information given in this section is for reference use only.

4.2.1 Specifications

Features

- Wide-VGA sensor (360, 960 pixels)
- Monochrome (VM-007-BW) or color (VM-007-COL)
- phyCAM-P – parallel interface
- Frame rate up to 60 fps
- Global shutter
- External Trigger and Strobe
- Multiplexer for on-the-fly 8- / 10-bit format selection (optional)
- LED light (optional)
- Secondary connector with trigger, strobe and I/O (optional)

Figure26: VM-007 (phyCAM-P with LED light, front / rear view)

Parameters

	VM-007-BW	VM-007-BW-MUX	VM-007-COL	VM-007-COL-MUX
Sensor				
Resolution	WVGA	WVGA	WVGA	WVGA
Pixels (H x V)	752 x 480	752 x 480	752 x 480	752 x 480
Sensor Size	1/3" 4.51 x 2.88 mm	1/3" 4.51 x 2.88 mm	1/3" 4.51 x 2.88 mm	1/3" 4.51 x 2.88 mm
Pixel Size	6.0 x 6.0 µm	6.0 x 6.0 µm	6.0 x 6.0 µm	6.0 x 6.0 µm
Color / Monochrome	monochrome	monochrome	color	color
Technology	CMOS	CMOS	CMOS	CMOS
Image Sensor	Aptina MT9V022	Aptina MT9V022	Aptina MT9V022	Aptina MT9V022
Scan System	progressive	progressive	progressive	progressive
Shutter Type	global	global	global	global
Fame rate (fps)	up to 60 fps	up to 60 fps	up to 60 fps	up to 60 fps
Video Resolution	n/a	n/a	n/a	n/a
Responsivity	4.8 V/lux-sec	4.8 V/lux-sec	4.8 V/lux-sec	4.8 V/lux-sec
Max. Dynamic Range	>55 dB linear	>55 dB linear	>55 dB linear	>55 dB linear
High Dynamic Range	>80...100 dB	>80...100 dB	>80...100 dB	>80...100 dB
Exposure Time	programmable	programmable	programmable	programmable
Gain	x1...x4	x1...x4	x1...x4	x1...x4
AEC	auto or manual	auto or manual	auto or manual	auto or manual
AGC	auto or manual	auto or manual	auto or manual	auto or manual
Gamma Correction	-	-	-	-
White Balance/AWB	n/a	n/a	manual	manual
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe	Trigger / Strobe	Trigger / Strobe
ROI	yes	yes	yes	yes
Skipping	2x2 / 4x4	2x2 / 4x4	n/a	n/a
Mirror	programmable	programmable	programmable	programmable
Image Processor	-	-	-	-
LED Lightning	optional	optional	optional	optional
Special Functions	see section 4.2.5	see section 4.2.5	see section 4.2.5	see section 4.2.5
Electrical Interface				
Video Output Type	digital	digital	digital	digital
Interface	phyCAM-P	phyCAM-P	phyCAM-P	phyCAM-P
Data Format	8-/ 10-Bit parallel	8-/ 10-Bit parallel	8-/ 10-Bit parallel	8-/ 10-Bit parallel
Interface-Mode	Y8 / Y10	Y8 / Y10	8/10 Bit RGGB (Bayer)	8/10 Bit RGGB (Bayer)
Dataline-Shifting	-	yes	-	yes
Camera Config. Bus	I²C	I²C	I²C	I²C
Supply Voltage	3.3 V	3.3 V	3.3 V	3.3 V
Power Consumption	320 mW	320 mW	320 mW	320 mW
Pwr. Consumpt. Standby	100 µW	100 µW	100 µW	100 µW
Mechanical Parameters				
Lens Connector	none / M12 / C-CS	none / M12 / C-CS	none / M12 / C-CS	none / M12 / C-CS
Lens	-	-	-	-
Housing	-	-	-	-
Dimensions (mm)	34 x 34	34 x 34	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5	4 x M2.5	4 x M2.5
Color (housing)	-	-	-	-
Weight (PCB)	7 g	7 g	7 g	7 g
Operating Temperature	-25...85°C	-25...85°C	-25...85°C	-25...85°C
Connectors				
Data and Power	FFC 33-pin	FFC 33-pin	FFC 33-pin	FFC 33-pin
Trigger / Sync.	FFC + JST 3-pin	FFC + JST 3-pin	FFC / JST 3-pin	FFC + JST 3-pin
Iris	-	-	-	-
Special functions	-	-	-	-

n/a: not applicable. All parameters are subject to change.

Table 11: VM-007 (phyCAM-P) Parameters

Electrical Specifications (without LED light)

	Symbol	min.	typ.	max.	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operating Current	I_{CAM}		100	-	mA
Input high voltage	V_{IH}	V_{CAM} -0.5	-	V_{CAM} +0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Output high voltage	V_{OH}	V_{CAM} -0.7	-	-	V
Output low voltage	V_{OL}	-	-	0.3	V
Voltage Set Resistor	R_{31}	-	0	2	Ω
Operating Temperature	T_{OP}	-25	-	85	°C
Storage Temperature	T_{STG}	-25	-	125	°C

	Symbol	min.	typ.	max.	Unit
Master Clock Frequency	f_{MCLK}	13	-	27	MHz
Clock Duty Cycle	$dutycyle_{MCLK}$	45	50	55	%
MCLK to PCLK delay	t_{CP}	3	7	11	ns
PCLK to data valid	t_{PD}	-2	0	2	ns
PCLK to Sync high	t_{PVH}	-2	0	2	ns
PCLK to Sync low	t_{PVL}	-2	0	2	ns
Data Setup-Time	t_{SD}	14	16	-	ns
Data Hold Time	t_{HD}	14	16	-	ns
I²C Frequency	f_{I2C}	-	100	-	kHz

Data Formats

Monochrome (VM-007-BW):

- Y8 : 8-bit grey scale
- Y10: 10-bit grey scale

Color (VM-007-COL):

- RGGB (Bayer-Pattern) up to 10-bit color depth

Notes

- Any other desired lower color / grey scale resolution can be configured by using a reduced subset of the data lines. To configure this connect only the upper data lines (MSB) to the microprocessor interface. Some microprocessors also enable dynamic configuration of the camera interface input.
- The –MUX variant allows dynamic (on–the-fly) switching of the camera between Y8 and Y10 (see section 4.2.5.2)

Spectral Characteristics

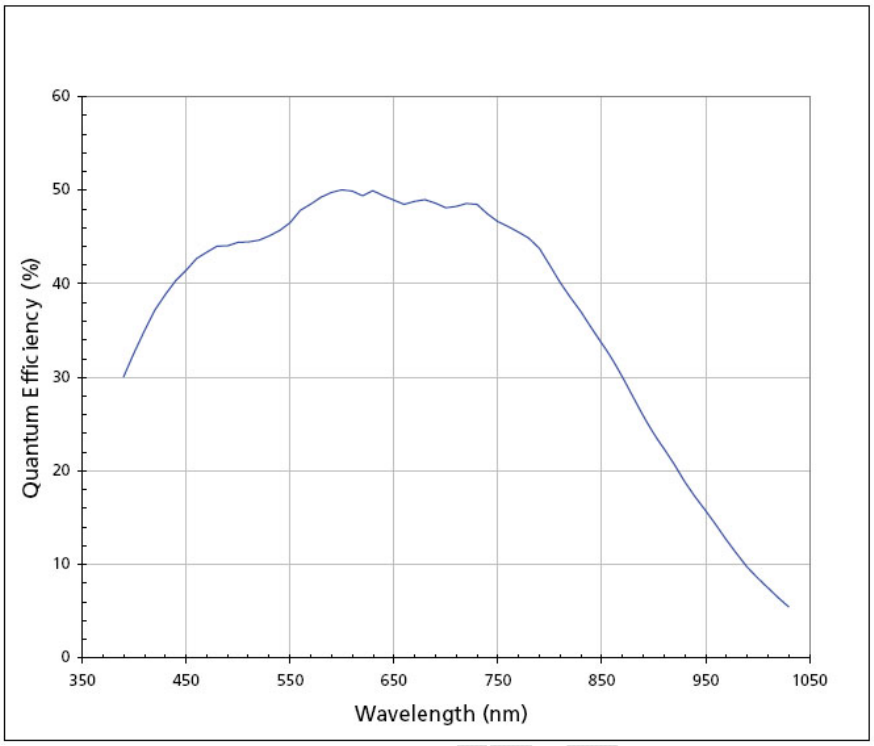


Figure27: phyCAM-P Spectral Characteristics (VM-007-BW)

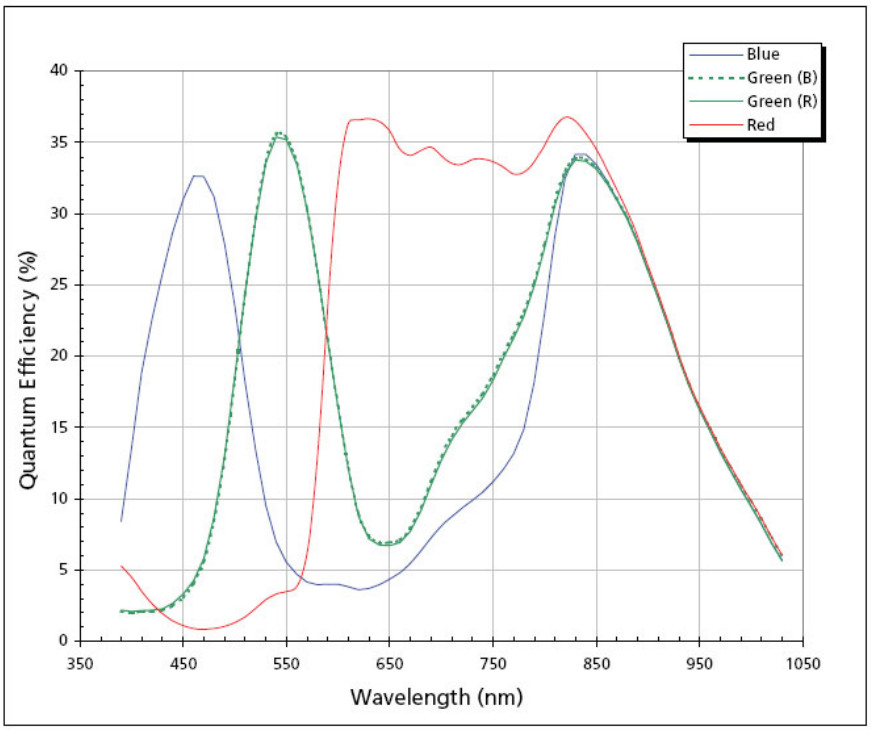


Figure28: phyCAM-P Spectral Characteristics (VM-007-COL)

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

4.2.2 I²C Addresses

Device	I²C-Address	Configuration			Variant
		CAM_CTRL1	J102	J101	
Camera Sensor	0x90	GND	**2-4**	**1-2**	all
		x	1-2		
	0x98	V_{CAM}	**2-4**	**1-2**	
		x	2-3		
	0xB0	GND	2-4	2-3	
		x	1-2		
	0xB8	V_{CAM}	2-4	2-3	
		x	2-3		
Bus-Multiplexer / LED	0x82				-MUX -LED

Default configuration (printed bold):
0x90 (CAM_CTRL1 = low)
0x98 (CAM_CTRL1 = high)

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with 7-bit Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

4.2.3 Feature Pins

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	**I²C-Adress-Select**	I	**J102:2-4, J104:NOMT**
		Strobe Output	O	J102:1-2 or 2-3, J104:0R
CAM_CTRL2	30	**GND**	-	**J103:1-2**
		Trigger Input	I	J103:2-3
CAM_RST	3	/Camera Reset	I	active low
CAM_OE	32	**Data Output Enable**	I	**R103=0R, R104=NOMT** active high
		n/a (open)	-	R103=NOMT, R104=0R

Notes:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

4.2.4 Jumper Map

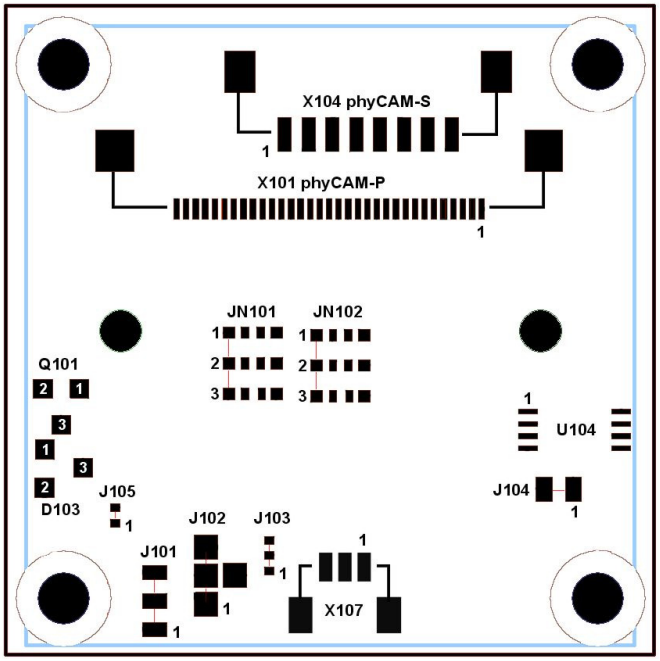


Figure29: VM-007 Jumper Map (PCB revision: PL1331.1)

4.2.5 Special Features

4.2.5.1 Windowing / Binning

To reduce the image resolution two functions of the camera can be used: Windowing and Binning. Which method is to be preferred depends on the application.:

- *Windowing:*
  Also called *Region of Interest* (ROI).
  Only a part of the sensor's pixel array is used for image aquisition. Pixels outside of this field are skipped. This method reduces the effecive size of the image sensor. This has to taken into consideration for calculation of the lens parameters focal length / angel of view.
  The origin of the ROI can be moved on the physical area of the image sensor. This allows electronical pan and tilt effects.
- *Binning:*
  Binning combines neighborhood pixels to one big pixel. This means the effective size of a pixel is increased while the number of pixel on the sensor is decreased. Binning improves the sensitivity of the sensor because the of the enlargement of the pixel size.
  On most color sensors that use the Bayer Pattern model, neighboring pixels cannot be combined because they have different color filters. See the sensor datasheet if the sensor supports binning on a color matrix.

Note:
When binning mode is activated, the polarity of the pixel clock is inverted. Take care that the qualifying edge of the clock is matching on both the image sensor and the CPU interface.

4.2.5.2 Dataline-Shifting

This function is available with the –MUX option only.

Camera interfaces of various microprocessors use different data bus widths. For example, a processor might support an 8-bit or 10-bit

camera interface. Some processors allow software configuration of the bus width according the interface of the camera module and its underlying sensor.

In addition, a particular application might define the width of the data bus, since the width of the camera interface defines the color depth. A wider interface allows a more precise representation of the brightness or color information of a pixel.

Example: If an application demands a high color depth, such as 10-bit, all 10 data lines of the camera are connected to the microprocessor interface. If a standard resolution of 8-bit is sufficient, the lower 2 data lines of the camera are left unconnected. Only the upper 8 lines are wired to the microprocessor interface, connecting D2 of the camera to D0 of the microprocessor.

However, some applications might require both options. Therefore it is advantageous to switch between 8-bit and 10-bit mode during operation.

Example:
For a precise measurement application, 10-bit color depth is needed. On the other hand, the application might also feature a viewfinder option. For this, 8-bit mode is more convenient, because 8-bit mode does not need any data format conversion to send the data to the display.

Some microprocessors already feature a dynamic configuration of the interface format. For other processors that do not feature this – such as the Marvell PXA270/PXA320 - the –MUX feature allows dynamic configuration on the camera module.
With the –MUX option, an additional multiplexer on the camera module shifts the data lines by two (see *Figure30*). Therefore D[9..2] of the sensor are routed to D[7..0] of the interface. The multiplexer is controlled by I²C commands.

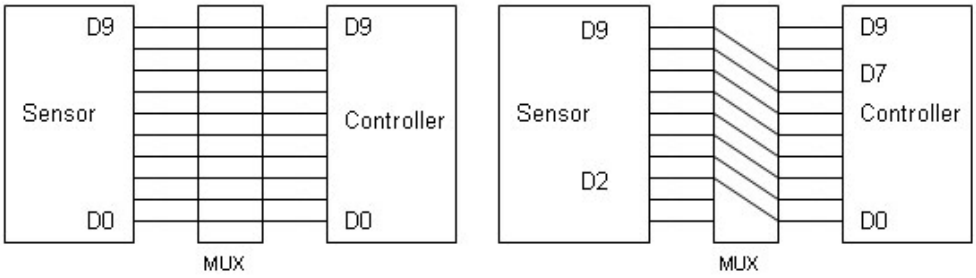


Figure30: Dataline-Shifting

Configuration of the data lines is done by data bit 0 of the I²C parallel port interface on I²C address 0x82, register address 0x01:

Data Bit	State	Function	Notes
0	0	10-bit image data	dataline-shifting not active (default)
0	1	8-bit image data	dataline-shifting active

Notes:

- The data direction of bit 0 must be set to output prior to using this function.
- Do not alter any other bits of the registers.
- Refer to the datasheet of the PCA9536 I²C port device for more information.

Registers:

Dataline-Shifting								
Device 0x82 – Register 0x00								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	-	TP101	LED	Dataline Shift

Dataline-Shifting – Data-Direction Register								
Device 0x82 – Register 0x03								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	-	DIR TP101	0	0

Assignment of data lines:

Image Data Out	Sensor Interface	
	Shifting not active	Shifting active
CAM_DD0	D0	D2
CAM_DD1	D1	D3
CAM_DD2	D2	D4
CAM_DD3	D3	D5
CAM_DD4	D4	D6
CAM_DD5	D5	D7
CAM_DD6	D6	D8
CAM_DD7	D7	D9
CAM_DD8	D8	D8
CAM_DD9	D9	D9

4.2.5.3 Trigger

Using the trigger input allows precise control of the point in time an image is captured by an electrical signal. The trigger signal is generated externally, not on the camera module, and is fed to the camera by the EXPOSURE input. The EXPOSURE signals can be used in several modes. See the Aptina MT9M022 or MT9V024 sensors datasheets for details. More information about snapshot mode can be found in the Aptina *TN0960_Snapshot* tech note.

Note: The EXPOSURE signal (*CAM_TRIG*) is available as of the phyCAM-P (part #: VM-007) PCB revision PL1331.0.

The trigger input is available at the pin *CAM_CTRL2* of the phyCAM-P connector (J103 has to be set to 2-3). This trigger input is also available at pin 1 of the extension connector X107.

4.2.5.3.1 Triggering in Snapshot-Mode

In snapshot mode, applying a high-level at the EXPOSURE input (CAM_TRIG) starts capturing an image (the CAM_TRIG signal is high-active).

At the beginning of a capture process, the image sensor starts the exposure of the image. The exposure time is set in the sensor register 0x0B. After the end of the exposure, the image data is output at the camera's data interface. This complete sequence is shown in *Figure31*.

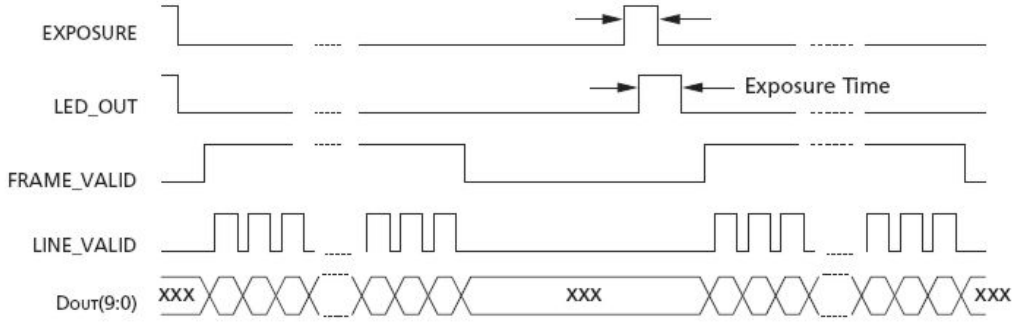
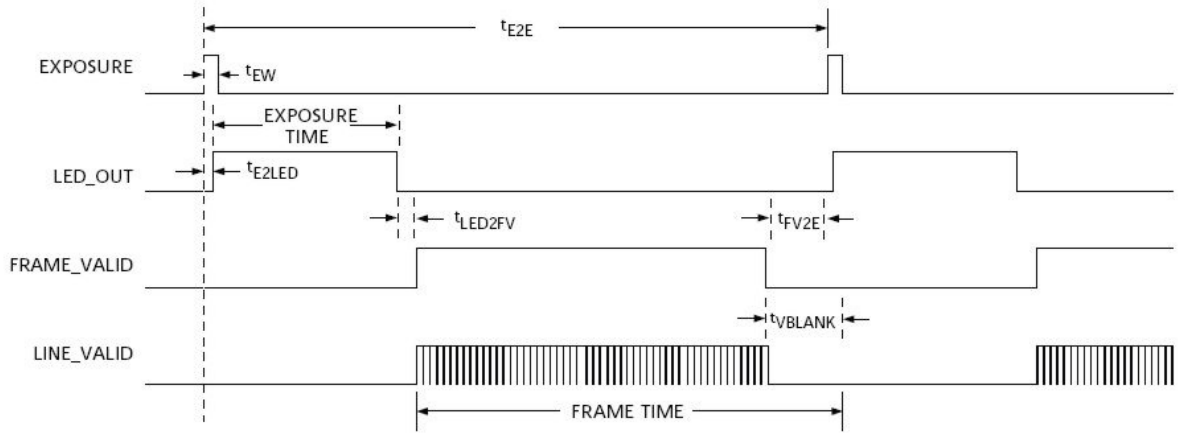


Figure31: CAM_TRIG (Exposure) and Exposure Time

If CAM_TRIG is held high beyond the end of the frame timing, a new capture is triggered. Thus, both single shots and image sequences can be achieved. A pulse on the CAM_TRIG input may not occur while a capture process is active.

After the end of the exposure time, the image data is output at the data lines of the camera interface (see *Figure32*).



Notes:
1. Not drawn to scale.
2. Frame readout shortened for clarity.
3. Progressive scan readout mode shown.
4. $t_{LED2FV} + t_{FV2E} + t_{E2LED} = t_{VBLANK} + t_{LEDOFF}$.

Reference: Aptina TN0960.fm – Rev.B 8/06 EN

Figure32: phyCAM-P Timing Snapshot-Mode (VM-007)

Symbol	Description	Value
t_{E2E}	EXPOSURE signal period	EXPOSURE TIME + FRAME TIME + t_{LEDOFF} (MIN)

t_{EW}	EXPOSURE signal pulse width	1 SYSCLK-cycles (MIN)
t_{E2LED}	EXPOSURE to LED_OUT	1 row-time
t_{LED2FV}	LED_OUT to FRAME_VALID	5 row-times + 25 SYSCLK-cycles
t_{FV2E}	FRAME_VALID to EXPOSURE	[R0x06 -4] row-times - 21 SYSCLK-cycles (MIN)
t_{VBLANK}	Vertical blanking time	R0x06 row-times + 4 SYSCLK-cycles
t_{LEDOFF}	Required time between successive exposures (not shown in *Figure32*)	2 row-times + 4 SYSCLK-cycles (MIN)

Notes: 1. See “Row-Time Definition” on TN0960 for the row-time unit definition.
2. SYSCLK-cycle unit is defined as the reciprocal of the SYSCLK input frequency.
3. To change exposure time, change the total shutter width register (R0x0B).
4. To change frame rate, change the t_{E2E} value

The following registers must be configured to activate the snapshot mode:

Register	Name	Bit	Bit Name	Bit Description	Value
0x07	Chip control	3	Sensor master / slave mode	0 = slave mode 1 = master mode	1
0x07	Chip control	4	Sensor snapshot mode	0 = snapshot disabled 1 = snapshot mode enabled	1
0x07	Chip control	5	Stereoscopy mode	0 = stereoscopy disabled 1 = stereoscopy enabled	0
0x07	Chip control	6	Stereoscopic master / slave mode	0 = stereoscopic master 1 = stereoscopic slave	0
0x07	Chip control	8	Simultaneous / sequential mode	0 = sequential mode 1 = simultaneous mode	1
0x20	Reserved	2	CR enable	0 = normal operation 1 = CR enabled	1
0x20	Reserved	9	RST enable	0 = normal operation 1 = RST enabled	1
0xAF	AGC/AEC enable	0	AEC enable	0 = disable AEC 1 = enable AEC	0

Table 12: VM-007 Configuration Snapshot-Mode

The functions “automatic black level correction” and “automatic gain correction” are optimized for continuous capture modes. In snapshot mode, these functions should be set to manual mode (*black-level* register 0x47 bit 0 = “1”, *gain* register 0xAF bit 1 = “0”)

The Linux camera drivers from PHYTEC feature the selection between snapshot and master mode (default) from driver version V2.6.31.

Due to the structure of the *GStreamer* framework, the samples provided for GStreamer are not compatible with the snapshot mode.

Please refer to the sensor datasheet for more information.

4.2.5.3.2 Configurations of the Trigger Input

The CAM_TRIG signal is tied to low by a 4.7 kΩ resistor on the camera module. To release a trigger pulse, the signal must be driven to high state, V_{CAM} (3.3V). CAM_TRIG is available at the connectors listed below (from PCB revision PL1331.1):

(a) at connector X101
The EXPOSURE signal (CAM_TRIG) can be routed to the CAM_CTRL2 pin (pin 30, X101) of the FFC connector. In default configuration, CAM_CTRL2 is tied to ground (GND). If CAM_CTRL2 is intended to be used as the trigger input, jumper J103 on the camera module is to be set to 2-3 position:

Signal	Pin	Function	I/O	Configuration
CAM_CTRL2	30	**GND**	-	**J103:1-2**
		Trigger Input	I	J103: 2-3

Important note:
The CAM_TRIG function is an input signal. Before connecting the camera, please ensure that the corresponding Carrier Board or target hardware application board supports this function and is properly configured.

On PHYTEC Carrier Boards, *CAM_CTRL2* is connected to GND by default. Confirm the configuration options before connecting the *EXPOSURE* signals via X101 on the phyCAM board.

(b) at the connector X107
The *CAM_TRIG* signal is also available at the connector X107. This allows the connection of external trigger sources directly to the camera module.

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	LED_OUT / STROBE

Table 13: VM-007 X107 Connector

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

Note: We recommend using only one trigger input connection option at a time.

4.2.5.4 Strobe / LED-OUT

The *Strobe / LED-OUT* output indicates the period of time when the sensor is undergoing exposure. When exposure is active, this output is active high.

The signal is active during the complete period of sensor exposure (exposure time). This is the period of time the sensor is sensitive to light. Depending on whether the current exposure time is greater or less than the required readout time of the frame, there are two slightly different timing patterns (*Figure33*).

Note that the data can be read only in the following frame. Exposure and readout of a specific frame are thus in different frames.

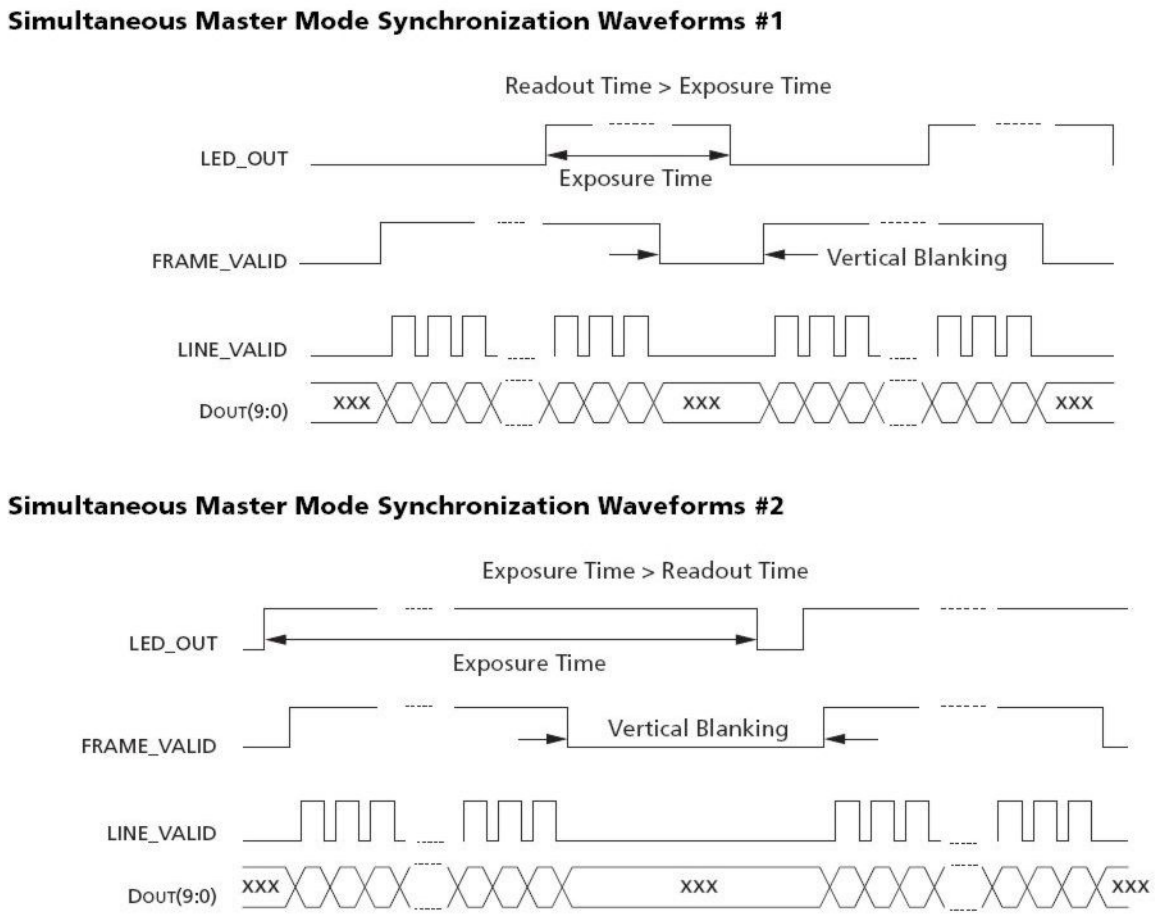


Figure33: VM-007 Timing Strobe/LED-OUT

The signal is available at the following connectors:

- *CAM_CTRL1* - pin 7 of the phyCAM-P connector (optional, depending on the configuration of the camera module)
- Pin 3 of the extension connector X107
- The signal can directly control the LEDs on the camera module (optional)

4.2.5.4.1 Configuration of the Strobe Signal

The *LED_OUT* signal can be activated in the sensor register 0x1B. Furthermore, the polarity of the signal can be set as follows:

Register, 0x1B, LED_OUT		
Bit 0	Disable LED_OUT	Disable LED_OUT output. When cleared, the output pin LED_OUT is pulsed high when the sensor is undergoing exposure
Bit1	Invert LED_OUT	Invert polarity of LED_OUT output. When set, the output pin LED_OUT is pulsed low when the sensor is undergoing exposure

The Linux camera drivers provided by PHYTEC activate the *LED_OUT* signal by default in high-active state. Please refer to the datasheet of the camera sensor for more information about the *LED_OUT* signal.

Note: The *LED_OUT* signal is available from PCB version PL1331.0.

4.2.5.4.2 Control of external light sources

The *Strobe/LED_OUT* signal is available at the connectors listed below (from PCB revision PL1331.1):

(a) at connector X101 (phyCAM-P)
The phyCAM-P interface features multipurpose pins that can be configured for different features. The phyCAM-P can be configured in a way that *Strobe/LED_OUT* is routed to the *CAM_CTRL1* pin (pin 7, X101 of the FFC connector). In the default configuration *CAM_CTRL1* is routed to the *CAM_ADR0* signal. If CAM_CTRL1 is intended to be used as Strobe/LED_OUT, the following jumpers must be set:

- J102 to 1-2 position
- J104 must be closed

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	**I²C-Adress-Select**	I	**J102:2-4, J104:NOMT**
		Strobe Output	O	J102:1-2 or 2-3, J104:0R

Important Note:
The *Strobe/LED_OUT* signal is an output signal. Before connecting the camera, please ensure that the corresponding Carrier Board or target hardware application board supports this function and is configured properly. The *CAM_CTRL1* pin of must be configured as an input. Otherwise, the camera module might be damaged when connected.

CAM_CTRL1 of PHYTEC Carrier Boards is connected to GND by default. Therefore camera modules that are configured so that *LED_OUT* is routed to *CAM_CTRL1* may **not** be connected to a standard PHYTEC Carrier Board.

(b) at the connector X107
The LED_OUT signal is also available at the connector X107. This allows the connection of gated light sources directly to the camera module.

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	LED_OUT / STROBE

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

Note: We recommend using only one connection option at a time.

4.2.5.4.3 Controlling the internal LEDs by STROBE

The VM-007-xxx-LED variant feature two red 5 mm LEDs (approx. 10.000 mcd, 630 nm). These LEDs can be controlled directly by the *Strobe/LED-OUT* signal. This function can be deactivated either by hardware (open jumper J105) or by software (disable *LED_OUT Bit 0*, Reg 0x1B of the camera sensor).

4.2.5.5 Reset

Applying a low-level (GND) at the reset input initiates a reset of the camera sensor. All registers are set to their default values. The reset input should be connected to the /RESET output of the

microcontroller board. The reset signal must be held on high-level during operation of the camera module.

Note: The reset input does not reset either the I²C I/O port device nor the multiplexer (-MUX option).

4.2.5.6 Output-Enable

The output-enable input allows control of the data lines CAM_DD[0...9]. Applying a high-level to this input will tristate these outputs. For normal operation, output enable must be at low-level (GND). The output enable feature is not available with the –MUX version.

Notes:
The sync signal outputs are not controlled by this signal.
The camera module can be configured in a way that the outputs are always active (see section 4.2.3).

4.2.5.7 LED Light

The phyCAM part # variants VM-007-xxx-LED feature two red 5-mm LEDs with a brightness approx. 10.000 mcd and a wavelength of 630 nm. These LEDs can be used to light objects close to the camera, such as barcode labels.

Note:
The LED light is available in both the phyCAM PCB version as well as the phyCAM M12 lens holder versions.

The LEDs can be controlled by the following methods:

(a) automatic control by the Strobe/LED_OUT - signal
The LEDs are controlled directly by the LED_OUT signal generated by the camera sensor. Thus, they are automatically switched on during the exposure time period and switched off at all other points in time.

- During live image capture, the LEDs are continuously flashing.
- In single shot mode, the LEDs flash shortly when an image acquisition is triggered.

- This method saves energy, as the LEDs are only operating during the exposure periods.

Read more about this mode in section 4.2.5.4.3.

(b) manual control

The LEDs can be controlled manually by the I²C-GPIO expander (option) on the camera module. Control is achieved by software commands via the I²C channel. The LEDs can be switched on or off. For manual control, automatic control by LED_OUT must be disabled. This can be done either by:

- Hardware: open J105 on the camera module
- Software: disable LED_OUT, bit 0, Reg 0x1B

The LED light is switched by bit D1 of the I²C port device:

LED-Light (manual)								
Device 0x82 – Register 0x00								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	-	TP101	LED	Dataline Shift

LED-Light (manual) – Data-Direction Register								
Device 0x82 – Register 0x03								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	-	-	-	-	-	DIR TP101	0	0

Notes:

- The data direction of bit D1 must be set to output prior to using this function.
- Do not alter any other bits of the registers.
- Refer to the datasheet of the PCA9536 port device for more information.

4.2.6 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website

for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

4.3 VM-008 - phyCAM-Analog Video Digitizer

Wide-VGA / monochrome, color

Note: This section describes the VM-008 video converter which features both phyCAM-P and phyCAM-S interface

4.3.1 Specifications

Features

- Wide-VGA
- monochrome, color
- 4 inputs for analog video sources
- Various input configurations:
  4 x CVBS (Composite) or
  3 x CVBS (Composite) and 1 x S-Video
- PAL and NTSC video standard
- Video processor: Brightness, hue, saturation, contrast and sharpness programmable by software
- Integrated scaler
- phyCAM-S – serial interface connector
- phyCAM-P – parallel interface connector
- Frame rate 25 fps (PAL) / 30 fps (NTSC)
- Status LEDs on all inputs, controllable by application software via I^2C interface
- Integrated 4 Kbit EEPROM for application specific data (read / write access via I^2C interface)
- Optional power supply rail for integrated power supply to the cameras.

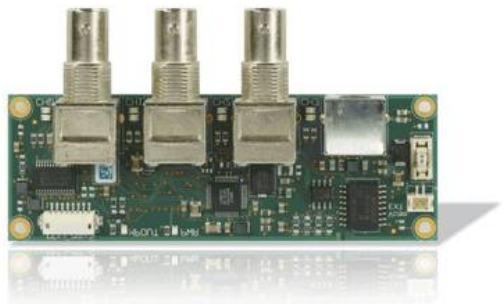


Figure34: Analog Video Digitizer (VM-008, PCB revision: PL1353.1)

Parameters

Function	VM-008
Video Converter	
Resolution	(W)VGA
Pixels (H x V)	720 x 576 (PAL) 720 x 480 (NTSC)
Sensor Size	n/a
Pixel Size	n/a
Color / Monochrome	color and monochrome
Technology	n/a
Digitizer	Techwell 9910
Scan-System	interlaced
Shutter-Type	n/a
Frame rate (fps)	25 fps (PAL) 30 fps (NTSC)
Composite Inputs	3 (+1)
S-Video Inputs	1
Special Functions	Parameter EEPROM 4kBit
	Status LED 4x red, 4x green

Electrical Interface	
Video Output Type	digital
Interface	phyCAM-P and phyCAM-S
Data Format	8-Bit parallel / 8-Bit serial
Interface-Mode	YCrCb 4:2:2 (ITU-R 601 / ITU-R656)
Dataline-Shifting	-
Camera Config. Bus	I²C
Supply Voltage	3.3V
Power Consumption	315 mW (digitizing)
Pwr. Consumpt. Standby	106 mW (power-down mode)

Mechanical Parameters	
Dimensions (mm)	100 x 34
Mounting	4 x M2.5
Color (housing)	-
Weight (standard variant)	70 g
Operating Temperature	-25...70°C

Connectors	
Video Inputs (depending on variant)	3 x BNC, 1 x Mini-DIN 4
	4 x BNC (composite)
	4 x Mini-DIN 6 (Multifunction)
Data and Power	FFC 33-pin (phyCAM-P)
	Hirose DF13A 8-pin (phyCAM-S)
Ext. Power Input for cameras	JST B2B-ZR-SM3 (2-pin)

n/a: not applicable. All parameters are subject to changes.

Table 14: VM-008 (Analog Video Digitizer) Parameters

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	3.15	3.3	3.6	V
Operating Current	I_{CAM}	-	95	120	mA
Digital Input high voltage	V_{IH}	2.0	-	V_{CAM}	V
Digital Input low voltage	V_{IL}	-	-	0,8	V
Output high voltage	V_{OH}	2.4	-	V_{CAM}	V
Output low voltage	V_{OL}	-	0.2	0,4	V
Voltage Set Resistor	R_{31}	-	0	2	Ω
Video Input Amplitude	$V_{VIDEO\ IN}$	0.5	1.00	1.40	V
Video Input Impedance	-		75		Ω
Camera Supply Voltage	V_{AUX}	-	-	14	V
Camera Supply Current	$V_{AUX\ (TOTAL)}$	-	-	1000	mA
Operating Temperature	T_{OP}	-20	-	85	°C
Storage Temperature	T_{STG}	-20	-	85	°C

	Symbol	Min.	Typ.	Max.	Unit
PCLK	f_{PCLK}	24	27	30	MHz
PCLK Duty Cycle	-	-	-	55	%
PCLK to data valid	t_{PD}	-	5	-	ns
I²C Clock Frequency	f_{I2C}	-	-	400	kHz

	Symbol	Min.	Typ.	Max.	Unit
LVDS Serializer					
Output differential voltage	$\|V_{OD}\|$	200	270	-	mV
V_{OD} change between complementary out states	$\|DV_{OD}\|$	-	-	35	mV
Output offset voltage	V_{OS}	0.78	1.1	1.3	mV
V_{OS} change between complementary out states	DV_{OS}	-	-	35	mV
Output current when short to GND	I_{OS}	-	±30	±40	mA
Output current in Tri-State	I_{OZ}	-	±1	±10	µA
LVDS-Receiver *)					
Shunt Resistance	R_{SHUNT}	-	100	-	Ω

*) board does not have LVDS clock input, shunt for compatibility reasons.

Data Formats

Monochrome:

- Y8 (processed): 8-bit grey scale

Color:

- YCrCb 4:2:2 (ITU-R 601 / ITU-R 656)

Note:
Color mode is automatically switched off and Y8 data format is output for low color amplitude signals, black and white video or very noisy signals, color

4.3.2 Functional Overview, Block Diagram

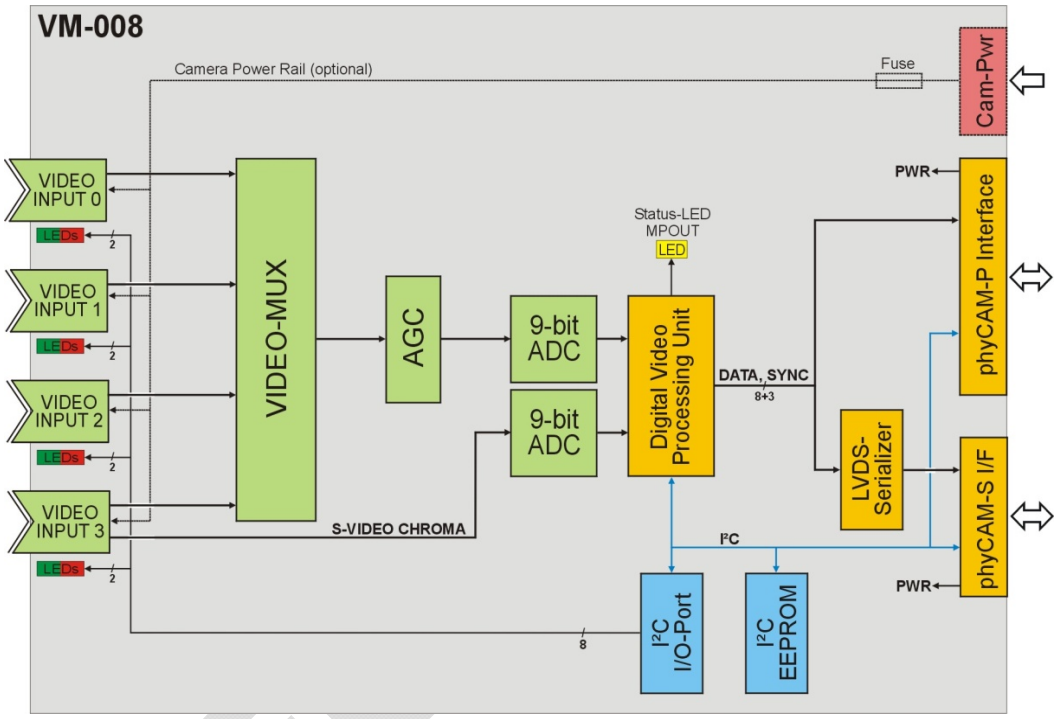


Figure35: VM-008 Analog Video Digitizer Block Diagram

The Analog Video Digitizer (AVD) module features 4 inputs for analog video sources. Video inputs can be configured in various ways. It can connect to up to four composite (CVBS) sources or three composite sources and one S-video source at input 3. According to the application requirements, the AVD module can be shipped with various input connectors.

Video signals feed to an internal analog source selector (multiplexer). The digitizer for composite signals is connected to the output of the source selector. The AVD module is capable of digitizing one source at a time. Channel selection is done by software. Channel 3 features either composite or S-video input. The luma component is fed by the source selector into the composite ADC, which digitizes the Y

component in this configuration. The chroma component is digitized by a separate A/D converter.

Additional signal processing is carried out fully digital by the video processing unit. This includes sync signal detection, Y/C separation, color demodulation, image correction, scaling / cropping and signal output formatting. The following parameters can be programmed, among others:

- Gain control (optional: AGC)
- Brightness, contrast, saturation, hue (NTSC only), sharpness
- Scaling and cropping (arbitrary downscaling ratios)
- Color- or monochrome format

Configuration registers are accessed via the I²C interface.

Digitized image data is available as a parallel data stream, at the phyCAM-P interface, and a serial LVDS data stream at the phyCAM-S interface. Image data consists of 8-bits pixel data, HSYNC, VSYNC and pixel clock. The data format is YCrCb 4:2:2 (compatible to ITU-R 601 or ITU-R 656). Only one data interface should be used at one time.

The AVD module offers the following additional features:

Internal Oscillator:
The ADV module has an internal oscillator. It is not necessary to provide an external master clocks (MCLK).

LEDs:
Two LEDs (red / green) are located next to each video input connector. The LEDs can be controlled by the application software via the I²C interface and be used for status information, such as green = video signal present, red = channel selected for digitizing. Plastic light guides are available, which makes the LEDs visible at the front panel of a device.

An additional LED visualizes the status signal *MPOUT* of the video processor. Various status information can be assigned to this signal by

software. The MPOUT signal is also available at the phyCAM-P – connector.

I²C-EEPROM:
Application data, such as parameters, can be stored in a serial EEPROM. Read and write accesses are done by the I²C-interface.

Power Supply:
As an option, the power supply of cameras connected to the module can be fed through the input connectors. This requires that the AVD module be populated with a 6-pin Mini-DIN "multifunction" connector. Two pins of these connectors are reserved for an external power supply, which is connected to the module by a 2-pin connector.

4.3.3 Video Inputs

All video inputs have an impedance of 75Ω. The video inputs can be populated with various connectors (*Table 15*).

Configuration	Input 0	Input 1	Input 2	Input 3
Configuration 1	Composite	Composite	Composite	Composite
	BNC	BNC	BNC	BNC
Configuration 2	**Composite**	**Composite**	**Composite**	**S-Video**
	BNC	**BNC**	**BNC**	**Mini-DIN 4**
Configuration 3	Composite+Pwr	Composite+Pwr	Composite+Pwr	Composite+Pwr
	Mini-DIN 6	Mini-DIN 6	Mini-DIN 6	Mini-DIN 6
Configuration 4	Composite+Pwr	Composite+Pwr	Composite+Pwr	S-Video+Pwr
	Mini-DIN 6	Mini-DIN 6	Mini-DIN 6	Mini-DIN 6

Composite = CBVS; Pwr = Power supply for camera / external video source

Table 15: VM-008 Analog Video Digitizer Video Input Configurations

The standard variant of the AVD module is equipped with connector configuration 2. Please inquire with the PHYTEC sales team for other configurations.

Input 3 can operate either in composite or S-video mode. Mode selection is done by software. For S-video, the AVD module must be populated with a 4-pin or 6-pin Mini-DIN connector.

Refer to section 0 for the location of the video connectors.

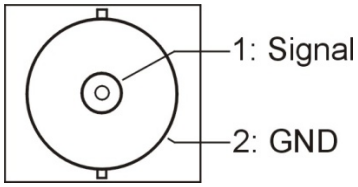


Figure36: BNC-connector

VM-008 - Composite Video Input (BNC Connector)			
Pin	Signal	Dir	Function
1	Composite Video In	IN	Composite (CVBS) Video Input
2	GND	-	Signal Ground

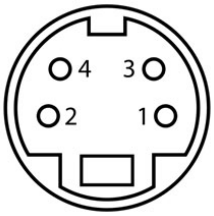


Figure37: Mini-DIN – connector 4-pin

VM-008 - S-Video Input (Mini-DIN Connector)			
Pin	Signal	Dir	Function
1	GND	-	Signal Ground
2	GND	-	Signal Ground
3	S_LUMA	IN	S-Video luma signal (Y) or Composite
4	S_CHROMA	IN	S-Video chroma signal (C) (channel 3 only)

View on socket (equivalent plug solder side)

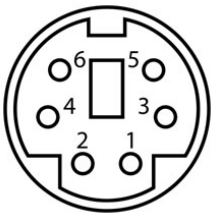


Figure38: Mini-DIN – connector 6-pin

VM-008 - Multifunction-Input (Mini-DIN Connector)			
Pin	Signal	Dir	Function
1	GND	-	Power Ground
2	V_CAM_EXT	OUT	Power Out – power supply for camera
3	GND	-	Signal Ground
4	GND	-	Signal Ground
5	S_LUMA	IN	S-Video luma signal (Y) or Composite
6	S_CHROMA	IN	S-Video chroma signal (C) (channel 3 only)

View on socket (equivalent plug solder side)

Note:
The S-video input is available at channel 3 only.
However, the *S_LUMA* – input can be used as a composite input at all channels.

4.3.4 VM-008 phyCAM Interfaces

The AVD module features both a phyCAM-P and a phyCAM-S interface:

- the phyCAM-P interfaces via the connector at X300, located on the bottom side of the AVD module PCB
- the phyCAM-S interfaces via the connector at X305, located on the top side of the AVD module PCB

Notes:
- Only one interface can be used at a time.
- *CAM_MCLK* signal of the phyCAM-P – interface is not used by the AVD module. Pin 29 of the connector X300 is not connected.
- The master clock channel of the phyCAM-S – interface is not used by the ADV module. The signal pair LVDS_CLOCK_P and LVDS_CLOCK_N is connected to a 100 Ω shunt for compatibility reasons. Feeding a clock signal to the AVD module is not necessary.

Image data is transmitted in 8-bit format. Two bytes of data are transmitted for one pixel. The first carries color information, the second transmits brightness (see *Figure39*).

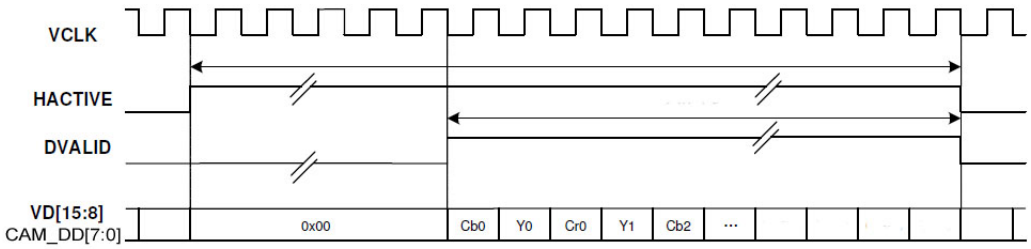


Figure39: VM-008 Analog Video Digitizer Data Format

Transmission starts with the blue color byte (Cb0), followed by the first brightness byte Y0. A sequence of four bytes contains the color information of one pixel and the brightness information of two pixels (YCrCb 4:2:2 format).

Please note that the video processor has to be set to 8-bit mode. In this mode, the lower data lines VD[7:0] of the video processor are not used. The upper data lines VD[15:8] are connected to the CAM_DD[7:0] output data lines

For more information about the video processor, please refer to the Techwell TW9910 datasheet.

4.3.5 I²C Addresses

Device	I²C-Address	Jumper Configuration
NTSC/PAL-Converter (TW9910)	0x8A	**J300: 1-2**
	0x88	J300: 2-3
LED Control (PCA9538)	0xE0	**J302: 2-3; J303: 2-3**
	0xE2	J302: 2-3; J303: 1-2
	0xE4	J302 :1-2; J303 :2-3
	0xE6	J302 :1-2; J303 :1-2
EEPROM Bank0 (M24C04)	0xA4	**J304: 1-2; J305: 2-3**
EEPROM Bank1 (M24C04)	0xA6	

The default configuration is printed bold:

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with 7-bit Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

Note:
The I²C address of the user EEPROM can be configured by the jumpers J304 and J305. This is helpful in case of address conflicts with other devices on the bus. See the table below for details.

Device	I²C-Address	Jumper Configuration	
		J304	J305
EEPROM Bank0 (M24C04)	0xA4	**1-2**	**2-3**
EEPROM Bank1 (M24C04)	0xA6		
EEPROM Bank0 (M24C04)	0xA0	2-3	2-3
EEPROM Bank1 (M24C04)	0xA2		
EEPROM Bank0 (M24C04)	0xA8	2-3	1-2
EEPROM Bank1 (M24C04)	0xAA		
EEPROM Bank0 (M24C04)	0xAC	1-2	1-2
EEPROM Bank1 (M24C04)	0xAE		

4.3.6 Feature Pins (phyCAM-P only)

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	Multi-Purpose Out	O	R314=0R: MPOUT-Signal **R314=NOMT: no connection**
CAM_CTRL2	30	not connected	-	open
CAM_RST	3	/Converter Reset	I	**R322=0R: Reset via CAM_RST** R322=NOMT: no Reset

pin numbers relate to X300.

Notes:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

4.3.7 Mechanical Dimensions/ Jumper Map

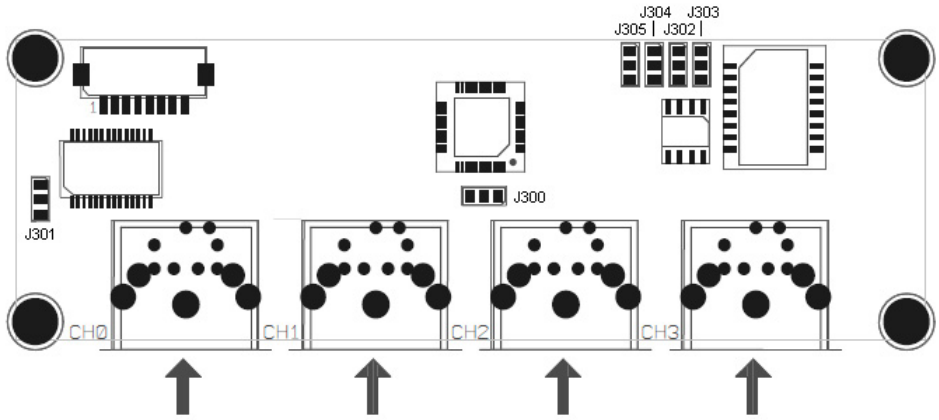
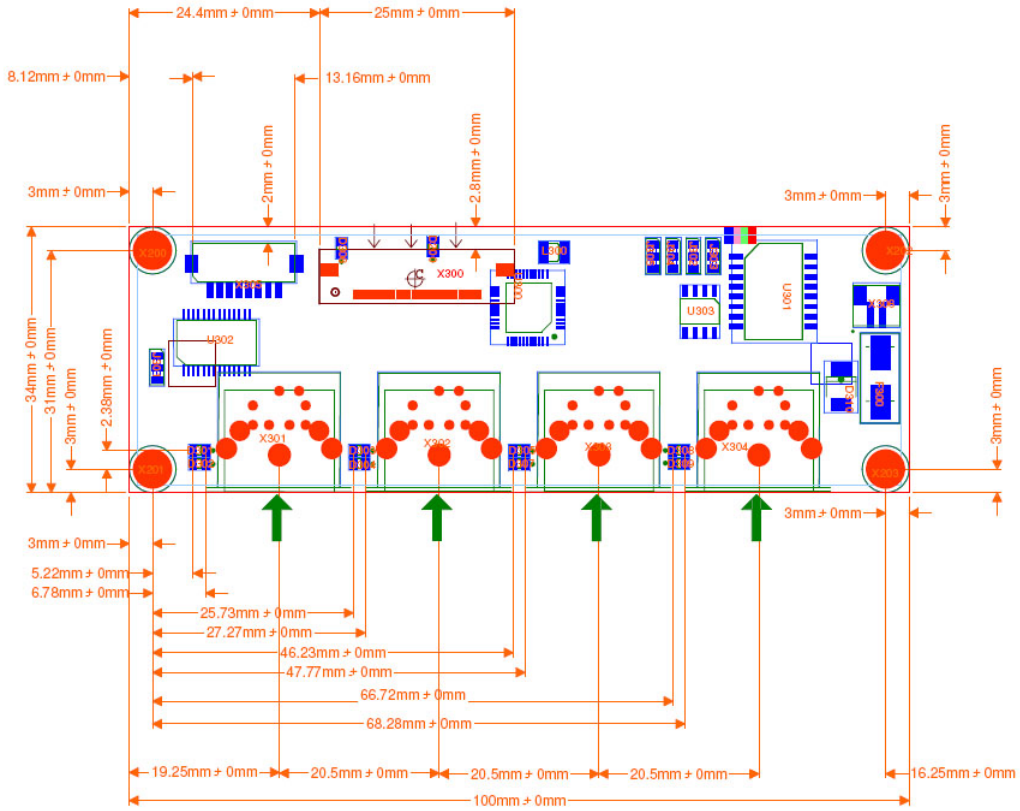


Figure40: VM-008 Jumper Map (PCB revision: PL1353.1)



Solder pads colors: blue= top side / red= bottom side (see section 2.3 for tolerances)

Figure41: VM-008 Mechanical Dimensions

4.3.8 Special Features

4.3.8.1 Power-LED

A green LED (D200) indicates active power supply to the AVD module. The LED is labeled *PWR* on the PCB.

4.3.8.2 Multi-Purpose Output

The multi-purpose output (*MPOUT*) of the video processor signals various status information. In standard configuration, the LED labeled MPOUT indicates the selected status information. MPOUT can also be fed to the *CAM_CTRL1* pin of the phyCAM-P- interface by mounting R314 with a 0 Ω resistor.

The MPOUT signal can configure the following (*Table 16*):

Signal	Description
Video Loss	1 = no video signal present on selected input. 0 = video signal present.
H-Lock	1 = H-Sync PLL is locked. 0 = H-Sync PLL is not locked.
S-Lock	1 = Sub-Carrier PLL is locked. 0 = Sub-Carrier PLL is not locked.
V-Lock	1 = V-Sync PLL is locked. 0 = V-Sync PLL is not locked.
MONO	1 = no color burst signal detected. 0 = color burst signal detected.
DET50	1 = 50 Hz – source detected. 0 = 60 Hz – source detected.
FIELD	1 = even field is being decoded. 0 = odd field is being decodes.
RTCO	real time control
0	(if RTSEL is set to 1111)

Table 16: Status Information on MPOUT (CAM_CTRL1)

The status LED *MPOUT* (D306) illuminates yellow if the signal is at active state (1).

Configuration of status information indicated by *MPOUT* can be set in register 0x19 (VBICNTL) of the video processor. Note that the highest bit of RTSEL is located in register 0x17.

Note:
Status information can also be queried by software via the I²C-interface (register 0x01 - Chip Status Register 1) of the video processor.

4.3.8.3 Status LEDs

A green and a red LED are placed next to each of the four video inputs. The LEDs are controlled by a GPIO port device via the I²C-interface. This allows the application software to display various status information, such as if a video signal is present at a certain input. The LEDs are located in a manner that allows optional use of plastic light guides so that the LEDs are visible at the front panel of the AVD module. For that, light guides manufactured by Mentor GmbH are recommended, as described below.

The LEDs are controlled by the I²C device “LED Control” (see *section 4.3.5*). To activate the LED function, all bits of the data direction register must first be cleared. The LEDs can subsequently be switched on / off by programming the bits of the output register.

Note:
A LED is switched on by clearing the corresponding bit of the control register:

Bit state	LED state
0	LED on
1	LED off (default)

LED-Control – Output Register								
Device 0xE0* – Register 0x01								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	LED CH2 RED	LED CH2 GREEN	LED CH2 RED	LED CH2 GREEN	LED CH1 RED	LED CH1 GREEN	LED CH0 RED	LED CH0 GREEN

LED-Control – Data-Direction Register								
Device 0xE0* – Register 0x03								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	0	0	0	0	0	0	0	0

*) default-address, see section 4.3.5

Please note that the data direction register defaults to 0xFF. Before using the LED function, the data direction register has to be programmed to 0x00.

The datasheet of PCA9538 provides more information about programming this device.

Plastic light guides can be used to visualize the LEDs at the front panel of the AVD module, next to the video input connectors. PHYTEC recommends the following spherical/planar and countersink light guides from Mentor GmbH, Erkrath, Germany: www.mentor-bauelemente.de.

The positions of the LEDs are optimized for the such light guides, which are easily mounted by press-insertion into the panel:

Spherical / Planar Version

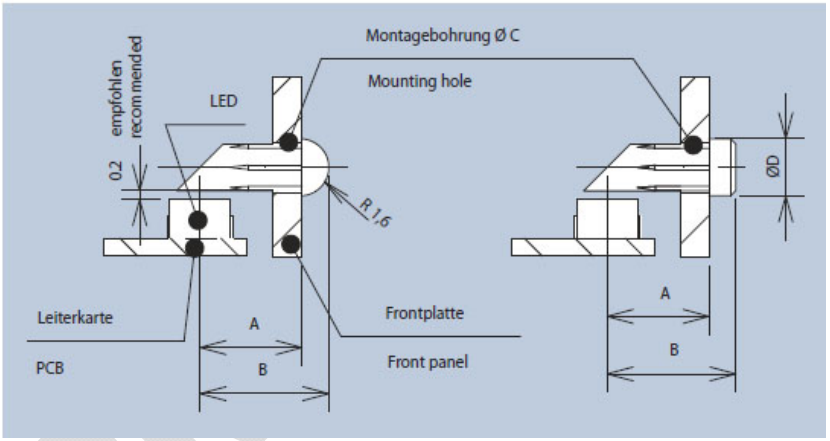


Figure42: Light Guides Example 1 (drawing: Mentor GmbH)

A	B	C	D	Type	Mentor – Part No.
5.7	7.2	2.8	3.2	spherical (*Figure42* - left)	1282.3000
5.7	7.2	2.8	3.2	planar (*Figure42* - right)	1282.4000

Countersink Version

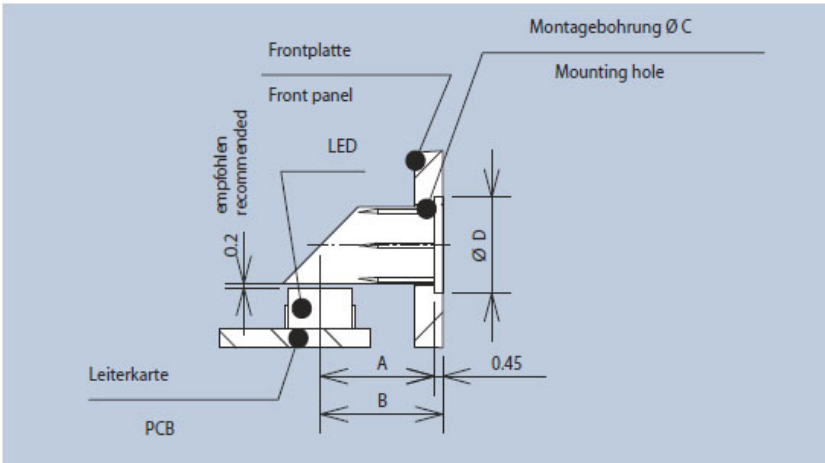


Figure43: Light Guides Example 2 (drawing: Mentor GmbH)

A	B	C	D	Type	Mentor – Part No.
6.2	6.6	2.8	3.2	countersink (*Figure43*)	1282.1200

4.3.8.4 EEPROM

The AVD module features an EEPROM that can store 4 Kb of application-specific data. This memory can be used for storage of configuration data, serial numbers, and other applicable uses.

The EEPROM is accessed via the I²C interface. The 4 Kb address range is divided into two banks. See *section 4.3.5* for the I²C device addresses of the two banks. Please note that other EEPROM devices might populate the Carrier Board or target hardware application board to which the AVD module is connected. If an address conflict occurs with other I²C devices on the same bus, the settings of the configuration jumpers J304 / J305 must be changed.

For more information about programming the EEPROM please see the M24C04 datasheet.

4.3.8.5 Power Supply for Video Devices

This option allows using a single wire connection for video sources that features both video signal and power supply for the video source.

To use this option, the AVD module must be populated with a 6-pin Mini–DIN connector. Power supply for the video sources is not generated on board the AVD module. A power source is connected to X306 of the AVD, which provides a supply voltage of up to 14 V DC for external video sources. Maximum input current is limited to 1A (all devices; current into X306).

The power source for the video devices is connected to X306:

Pin	Dir	Function
1	-	GND (Ground)
2	IN	Input Camera Supply Voltage (positive w/ respect to GND)

Connector type: JST B2B-ZR-SM3
Matching housing: JST ZHR-2

The external power supply is protected against reverse polarity by an internal diode and is buffered by a 10µF capacitor. A miniature fuse (F300) protects the external video source supply against over current. In standard configuration, the AVD module is shipped with a 1A fuse installed at F300. Alternatively, fuses with lower ratings can be installed.

The positive pin of the power source must be connected to pin 2 of X306. Pin 1 of the connector at X306 is internally connected to the signal ground of the video digitizer (GND). No potential difference may occur between the negative pin of the external power source for connected video devices and the GND potential of the video decoder.

4.3.9 Mounting Holes

If required, the mounting holes X200, X201, X202, X203 can be connected via capacitors or resistors to the GND plane of the AVD module. This might be useful to improve EMI behavior of the system. SMT components with 0805 footprint can be mounted at CB208, CB209, CB210 and CB211.

4.3.10 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

4.4 VM-009 - phyCAM-P camera module

1.3 Mpixels / color / SOC

4.4.1 Specifications

Features

- 1.3 megapixel image sensor, color
- phyCAM-P – parallel interface
- Frame rate up to 30 fps
- Rolling Shutter
- SOC – System on Chip: Integrated preprocessor
- RGB, YUV and RAW (Bayer pattern) output formats
- Integrated color- and gamma correction, sharpness enhancement, lens shade correction, digital zoom
- Automatic white balance (AWB) and auto black reference (ABR), auto flicker avoidance
- Fast exposure adaption
- Strobe output (fully automatic lightning control)
- Secondary connector for strobe output on the module (optional)

Figure44: phyCAM-P (VM-009) (front / rear view)

Parameters

	VM-009
Sensor	
Resolution	1.3 Mpixel
Pixels (H x V)	1280 x 1024
Sensor Size	1/3" 4.6 x 3.7 mm
Pixel Size	3.6 x 3.6 µm
Color / Monochrome	color
Technology	CMOS
Image Sensor	Aptina MT9M131
Scan System	progressive
Shutter Type	rolling
Frame rate (fps) full resolution	up to 30 fps
Video Resolution	n/a
Responsivity	1.0 V/lux-sec
Max. Dynamic Range	71 dB
High Dynamic Range	-
Exposure Time	programmable
Gain	programmable
AEC	yes
AGC	yes
Gamma Correction	yes
White Balance/AWB	yes / yes
Ext. Trigger / Sync.	Strobe
ROI	yes
Skipping	2 / 4
Mirror	programmable
Image Processor	yes
LED Lightning	-
Special Functions	sharpening, lens shade corr., color control...

Electrical Interface	
Video Output Type	digital
Interface	phyCAM-P
Data Format	8-/ 10-Bit parallel
Interface-Mode	YUV, RGB-565, RGB-555, RGB-444, Raw RGGB (Bayer, processed)
Dataline-Shifting	-
Camera Config. Bus	I²C
Supply Voltage	2.8 V
Power Consumption	170 mW
Pwr. Consumpt. Standby	TBD.

Mechanical Parameters	
Lens Connector	none / M12 / C-CS
Lens	34 x 34
Housing	4 x M2.5
Dimensions (mm)	7 g
Mounting	-25...70°C

Connectors	
Data and Power	FFC 33-pin
Trigger / Sync.	FFC + JST 3-pin

n/a: not applicable. All parameters are subject to change.

Table 17: VM-009 (phyCAM-P) Parameters

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	2.5	2.8	3.1	V
Operating Current	I_{CAM}	-	-	160	mA
Input high voltage	V_{IH}	2.0	-	V_{CAM}	V
Input low voltage	V_{IL}	-0.3	-	0.9	V
Output high voltage	V_{OH}	V_{CAM} -0.3	-	V_{CAM}	V
Output low voltage	V_{OL}	0	-	0.3	V
Voltage Set Resistor	R_{31}	215	220	224	Ω
Operating Temperature	T_{OP}	-25	-	70	°C
Storage Temperature	T_{STG}	-30	-	80	°C

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	-	-	54	MHz
Clock duty cycle	$dutycyle_{MCLK}$	40	50	60	%
MCLCK to PCLK delay	t_{CP}	7	9	15	ns
PCLK to data valid	t_{PD}	4	8	P	ns
PCLK to Sync high	t_{PVH}	4	8	P	ns
PCLK to Sync low	t_{PVL}	4	8	P	ns
Data Setup-Time	t_{SD}	4	8	P	ns
Data Hold Time	t_{HD}	4	8	P	ns
I²C Frequency	f_{I2C}	-	100	-	kHz

Note: P= ½ PCLK Period

Data Formats

Monochrome:

- Y8 (processed)

Color:

- YCrCb 4:2:2
- RGB 565 (16-bit)
- RGB 555 (15-bit)
- RGB 444 (12-bit)
- ITU-R BT.656 marker-embedded
- RGGB (by color processor processed Bayer format)
- RGGB (Bayer format, raw sensor data)

Note:

- Any other desired lower color / grey scale resolution can be configured by using a reduced subset of the data lines. To configure this, connect only the upper data lines (MSB) to the microprocessor interface.

Some microprocessors also enable dynamic configuration of the camera interface input.

Spectral Characteristics

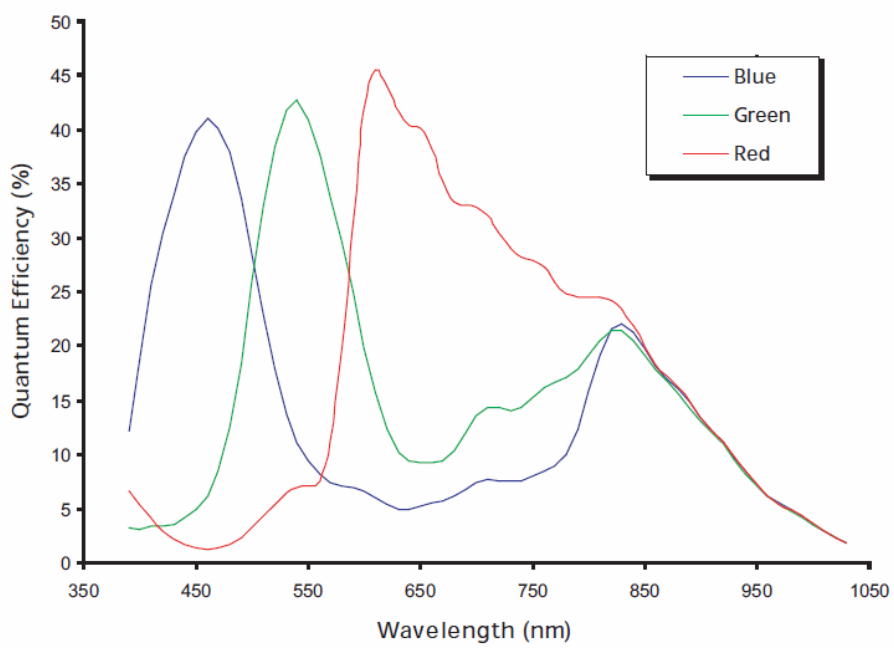


Figure45: VM-009 Spectral Characteristics

4.4.2 I²C Addresses

Device	I²C-Address	Configuration		Variant
		CAM_CTRL1	J101	
Camera Sensor	0x90	GND	2-4	all
		x	**1-2**	
	0xBA	V_{CAM}	2-4	
		x	2-3	

Default setting (printed in bold):
0x90 (J101: 1-2)

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with 7-bit Linux, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

4.4.3 Feature Pins

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	I²C-Adress-Select	I	J101:2-4, J102:NOMT
		Strobe Output	O	J101:1-2 or 2-3, J102:0R
		open	**-**	**J101:1-2 or 2-3, J102: NOMT**
CAM_CTRL2	30	Standby	I	J103:2-3 and J104:NOMT
		Without Standby	-	**J103:1-2**
CAM_RST	3	/Camera Reset	I	active low
CAM_OE	32	Data Output Enable	I	J105:2-3
		Always Enable	-	**J105:1-2**

Notes:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

4.4.4 Jumper Map

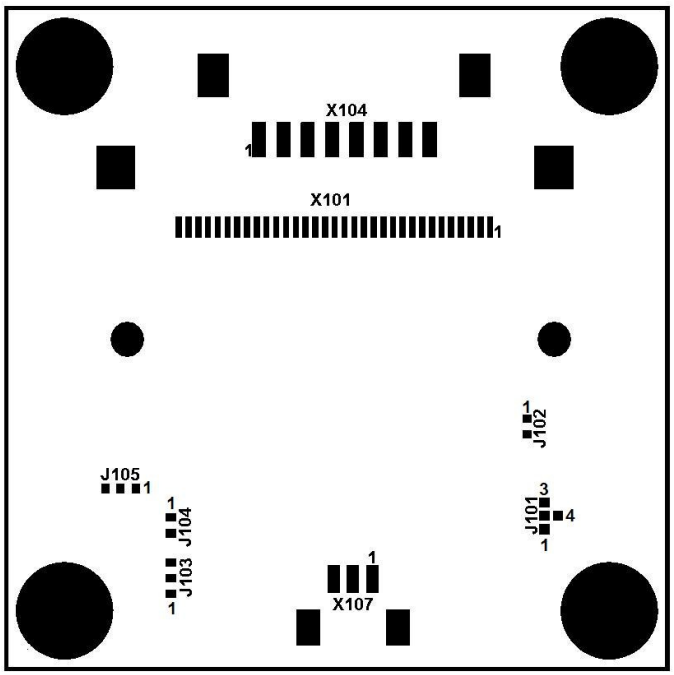


Figure46: VM-009 Jumper Map (PCB revision: PL1339.0)

4.4.5 Special Features

4.4.5.1 Strobe

The strobe signal indicates the period of time the sensor array is in exposure mode. The output is pulsed high when the pixel array is sensitive to light.

The signal remains active during the complete exposure period of the sensor. Two slightly different timing characteristics result from whether the current exposure time is greater or less than the required readout time of the frame (*Figure47*).

Please note that the image data is read out as indicated below. This shows that exposure and readout time of an image do not take place in the same frame.

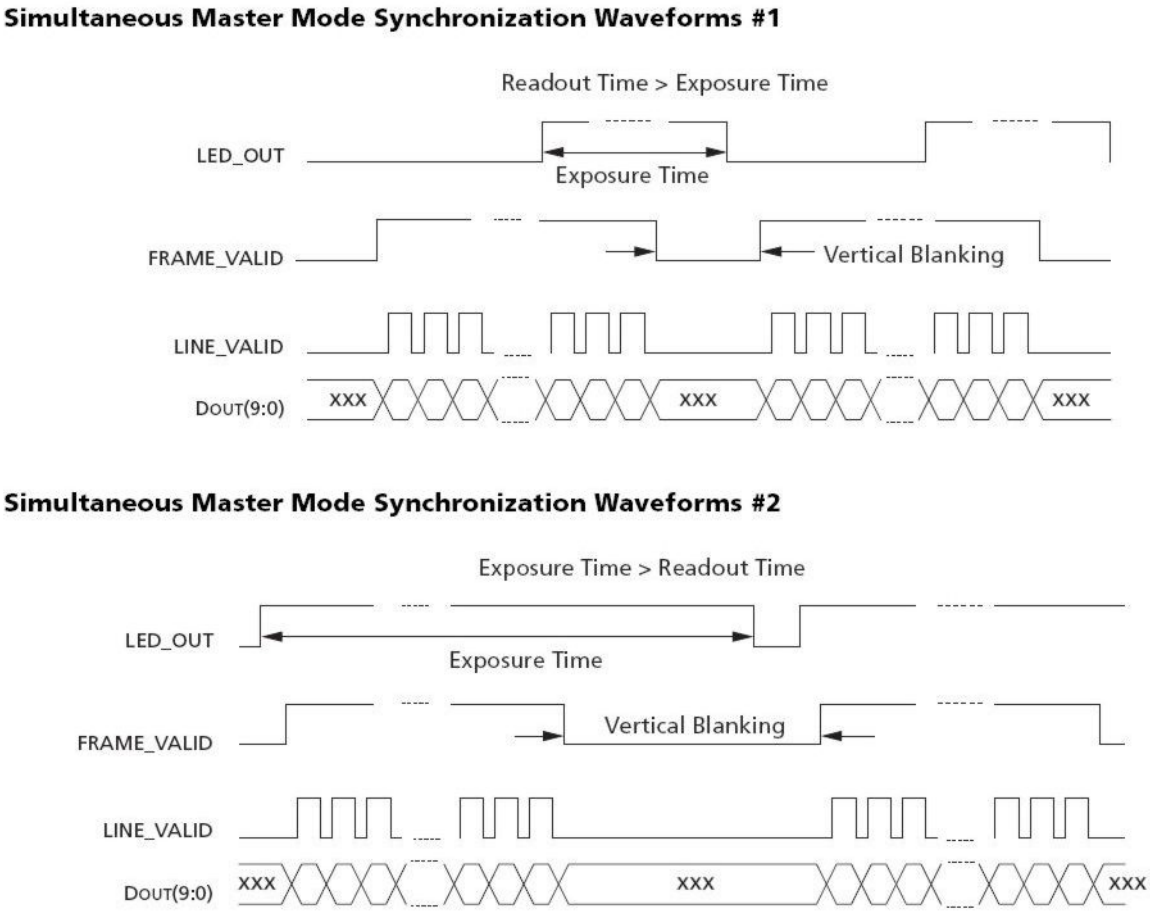


Figure47: phyCAM-P Timing Strobe/LED-OUT (VM-009)

The strobe signal is available on the following connectors:

- CAM_CTRL1 (pin 7) of the phyCAM-P – connector (optional, depending on the configuration of the module)
- Pin 3 of the extension connector X107

4.4.5.2 Reset

The reset signal of theVM-009 module is identical to the reset of the VM-007 camera module. Please refer to section 4.1.4.4.

4.4.5.3 Output-Enable

The output enable function of the of VM-009 module is identical to the reset of the VM-007 camera module. Please read section 4.1.4.5.

4.4.5.4 Image Processor

The integrated image flow processor (IFP) allows carrying out numerous pre-processing functions on the image on the camera module. Examples of these features include: gamma correction, color correction, sharpening, lens shading correction and on-the-fly defect correction.

Note:
Please refer to the datasheet of the camera sensor for detailed information.

4.4.6 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

Important Note:

- When using an Embedded Video Kit in conjunction with a SOM supporting a Freescale i.MX microprocessor, ensure sure that the kit Carrier Board PCB version is PL1280.5 or higher. Older Carrier Boards support 3.3V cameras only. Connecting a camera module to older PCB version Carrier Boards will cause damage to the camera module.
- The VM-009 camera module is not supported by PXA270 Video Kits. Connecting VM-009 camera module to PXA270 Carrier Boards will cause damage to the camera module.

Our sales team is ready to consult in selection of appropriate kits and image processing hardware.

4.5 VM-010 – phyCAM-P camera module
Wide-VGA / monochrome, color

4.5.1 Specification

Features

- Wide-VGA – sensor (360,960 pixels)
- Monochrome (VM-010-BW) or color (VM-010-COL)
- phyCAM-P – interface
- Frame rate up to 60 fps
- Global shutter
- External Trigger and Strobe
- Secondary connector with trigger, strobe and I/O (optional)

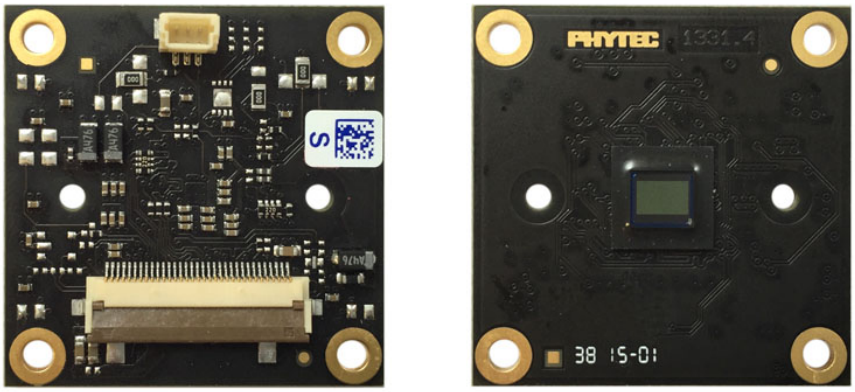


Figure48: VM-010 (phyCAM-P, PL1331.4) (rear / front view)

Note:
The following description refers to versions PL1331.4 and higher. If you have an older version of this camera module please contact Phytec support to obtain the corresponding version of the manual L-748e_9.

Parameters

	VM-010-BW	VM-010-COL
Sensor		
Resolution	WVGA	WVGA
Pixels (H x V)	752 x 480	752 x 480
Sensor Size	1/3" 4.51 x 2.88 mm	1/3" 4.51 x 2.88 mm
Pixel Size	6.0 x 6.0 µm	6.0 x 6.0 µm
Color / Monochrome	monochrome	color
Technology	CMOS	CMOS
Image Sensor	Aptina MT9V024	Aptina MT9V024
Scan System	Progressive	progressive
Shutter Type	global	global
Fame rate (fps)	up to 60 fps	up to 60 fps
Video Resolution	n/a	n/a
Responsivity	4.8 V/lux-sec	4.8 V/lux-sec
Max. Dynamic Range	>55 dB linear	>55 dB linear
High Dynamic Range	>100 dB	>100 dB
Exposure Time	programmable	programmable
Gain	x1...x4	x1...x4
AEC	auto or manual	auto or manual
AGC	auto or manual	auto or manual
Gamma Correction	-	-
White Balance/AWB	n/a	manual
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	yes	yes
Binning	2x2 / 4x4	n/a
Mirror	programmable	programmable
Image Processor	-	-
LED Lightning	-l	-
Special features	see section 4.5.5	see section 4.5.5

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-P	phyCAM-P
Data Format	8-/ 10-Bit parallel	8-/ 10-Bit parallel
Interface-Mode	Y8 / Y10	8/10-Bit RGGB (Bayer)
Dataline-Shifting	-	-
Camera Config. Bus	I²C	I²C
Supply Voltage	3.3 V	3.3 V
Power Consumption	165 mW	165 mW
Pwr. Consumpt. Standby	115 µW	115 µW

Mechanical Parameters		
Lens Connector	none / M12 / C-CS	none / M12 / C-CS
Lens	-	-
Housing	-	-
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	-	-
Weight (PCB)	7 g	7 g
Operating Temperature	-25...85°C	-25...85°C

Connectors		
Data and Power	FFC 33-pin	FFC 33-pin
Trigger / Sync.	FFC + JST 3-pin	FFC / JST 3-pin
Iris	-	-
Special functions	-	-

n/a: not applicable. All parameters are subject to change.

Table 18: Parameters VM-010 (phyCAM-P)

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operating Current	I_{CAM}	-	50	200	mA
Input high voltage	V_{IH}	V_{CAM} -1.4	-		V
Input low voltage	V_{IL}		-	1.3	V
Output high voltage	V_{OH}	V_{CAM} -0.3	-	-	V
Output low voltage	V_{OL}	-	-	0.3	V
Voltage Set Resistor	R_{31}	-	0	2	Ω
Operating Temperature	T_{OP}	-30	-	105	°C
Storage Temperature	T_{STG}	-30	-	105	°C

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	13	26.6	27	MHz
Clock Duty Cycle	$dutycyle_{MCLK}$	45	50	55	%
MCLK to PCLK delay	t_{CP}	4	6	8	ns
PCLK to data valid	t_{PD}	-3	0.6	3	ns
PCLK to Sync high	t_{PFLR}	5	7	9	ns
PCLK to Sync low	t_{PFLR}	5	7	9	ns
Data Setup-Time	t_{SD}	14	16	-	ns
Data Hold Time	t_{HD}	14	16	-	ns
I²C Frequency	f_{I2C}	-	100	400	kHz

Data Formats

Monochrome (VM-010-BW):

- Y8 : 8-bit grey scale
- Y10: 10-bit grey scale

Color (VM-010-COL):

- RGGB (Bayer-Pattern) up to 10-bit color depth

Notes

- Any other desired lower color / grey scale resolution can be configured by using a reduced subset of the data lines. To configure this, connect only the upper data lines (MSB) to the microprocessor interface. Some microprocessors also enable dynamic configuration of the camera interface input.
- The –MUX variant allows dynamic (on–the-fly) switching of the camera between Y8 and Y10 (see section 4.2.5.2)

Spectral Characteristics

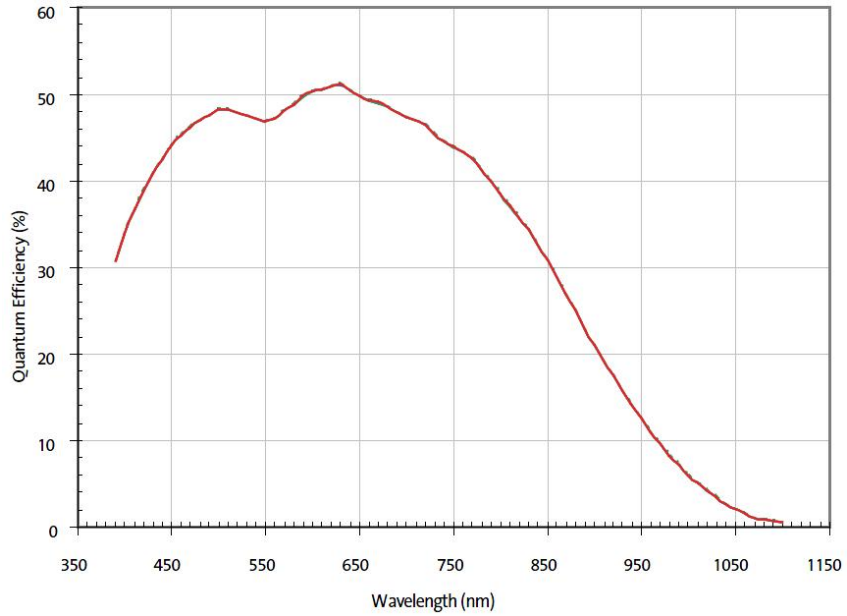


Figure49: Spectral Characteristics VM-010-BW

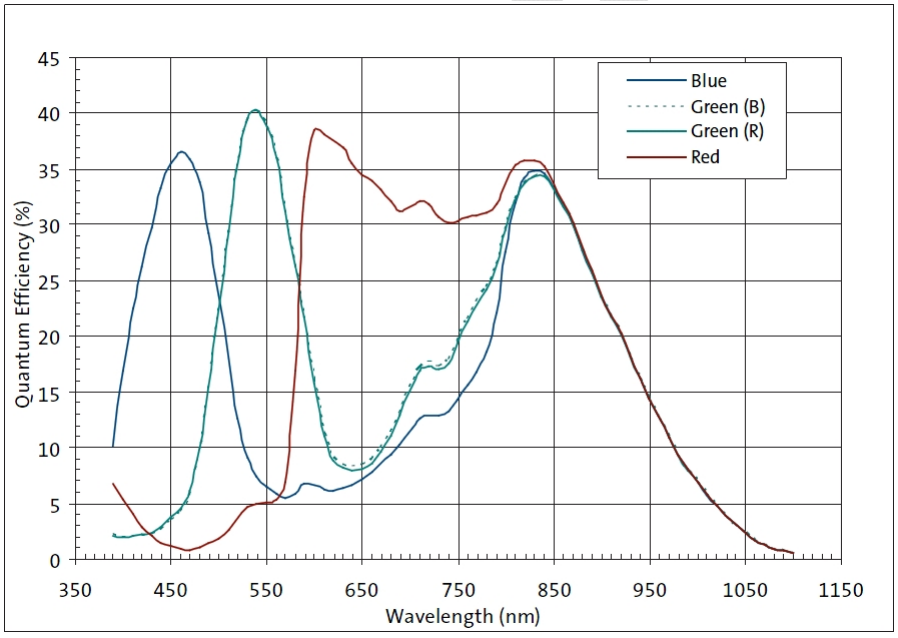


Figure50: Spectral Characteristics VM-010-COL

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

4.5.2 I²C Addresses

Device	I²C-Address	Configuration			Variant
		CAM_CTRL1	J102	J101	
Kamerasensor	0x90	GND	**2-4**	**1-2**	all (PL1331.4 and higher)
		x	2-3		
	0x98	V_{CAM}	**2-4**	**1-2**	
		x	1-2		
	0xB0	GND	2-4	2-3	
		x	2-3		
	0xB8	V_{CAM}	2-4	2-3	
		x	1-2		

Default configuration (printed bold):
0x90 (CAM_CTRL1 = low)
0x98 (CAM_CTRL1 = high)

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

4.5.3 Feature Pins

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	**I²C-Adress-Select**	I	**J102:2-4, J103:NOMT**
		Strobe Output	O	J102:1-2 or 2-3, J103:0R
CAM_CTRL2	30	**GND**	-	**J107: 2-4**
		Trigger Input	I	J107:2-3
		Standby	I	J107:1-2
CAM_RST	3	/Camera Reset	I	active low
CAM_OE	32	**Data Output Enable**	I	**R125=22R** active high, internal Pull-up to 3V3
		n/a (open)	-	R115=NOMT

Notes:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

4.5.4 Jumper Map

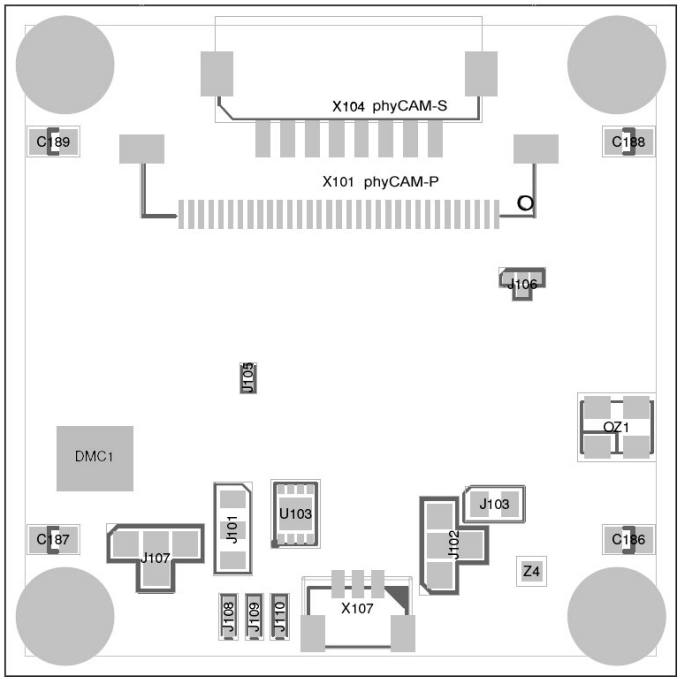


Figure51: VM-010 Jumper Map (PCB revision: PL1331.4)

4.5.5 Special Features VM-010

4.5.5.1 Windowing / Binning

To reduce the effective resolution of the sensor, windowing and binning can be used. The VM-010 module features the same methods as the VM-007. Please refer to section 4.2.5.1 for details.

4.5.5.2 Trigger

Using the trigger input allows precise control of the point in time an image is captured by an electrical signal. The trigger signal is generated externally, not on the camera module, and is fed to the camera by the EXPOSURE input. The EXPOSURE signals can be used in several modes. See the ON Semiconductor MT9V024 sensor's datasheets for details. More information about snapshot mode can be found in the *TN0960_Snapshot* tech note.

The trigger input is available at the pin *CAM_CTRL2* of the phyCAM-P connector (J107 has to be set to 2-3). This trigger input is also available at pin 1 of the extension connector X107.

4.5.5.2.1 Triggering in Snapshot-Mode

In snapshot mode, applying a high-level at the EXPOSURE input (CAM_TRIG) starts capturing an image (the CAM_TRIG signal is high-active).

At the beginning of a capture process, the image sensor starts the exposure of the image. The exposure time is set in the sensor register 0x0B. After the end of the exposure, the image data is output at the camera's data interface. This complete sequence is shown in *Figure31*.

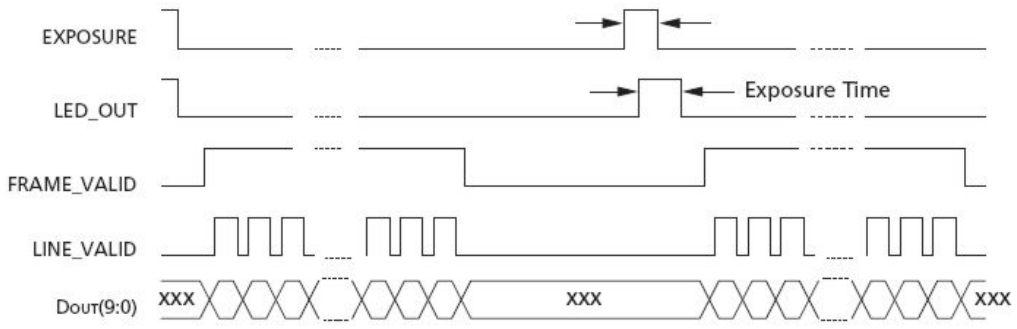
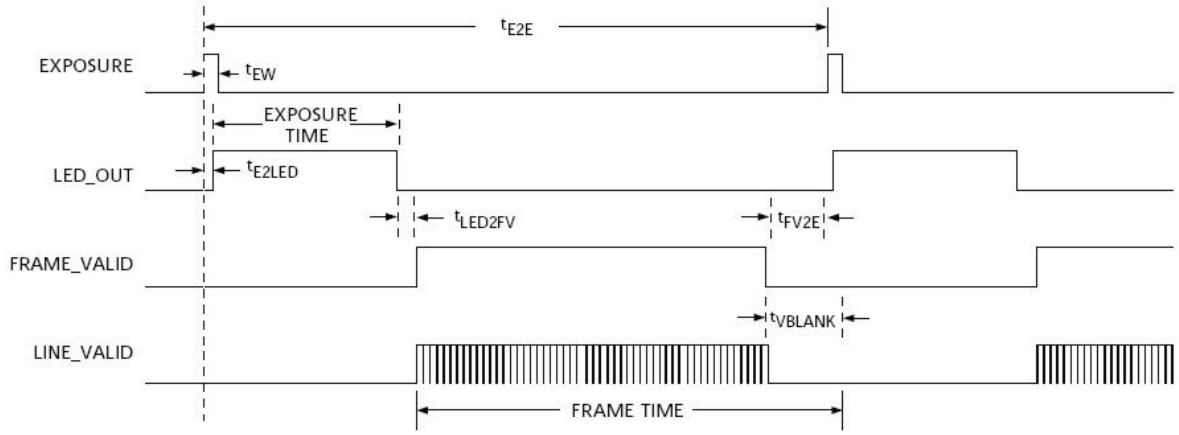


Figure52: CAM_TRIG (Exposure) and Exposure Time

If CAM_TRIG is held high beyond the end of the frame timing, a new capture is triggered. Thus, both single shots and image sequences can

be achieved. A pulse on the CAM_TRIG input may not occur while a capture process is active.

After the end of the exposure time, the image data is output at the data lines of the camera interface (see Figure53).



Notes:
1. Not drawn to scale.
2. Frame readout shortened for clarity.
3. Progressive scan readout mode shown.
4. $^{t}LED2FV + {}^{t}FV2E + {}^{t}E2LED = {}^{t}VBLANK + {}^{t}LEDOFF$.

Reference: Aptina TN0960.fm – Rev.B 8/06 EN

Figure53: phyCAM-P Timing Snapshot-Mode (VM-010)

Symbol	Description	Value
t_{E2E}	EXPOSURE signal period	EXPOSURE TIME + FRAME TIME + t_{LEDOFF} (MIN)
t_{EW}	EXPOSURE signal pulse width	1 SYSCLK-cycles (MIN)
t_{E2LED}	EXPOSURE to LED_OUT	1 row-time
t_{LED2FV}	LED_OUT to FRAME_VALID	5 row-times + 25 SYSCLK-cycles
t_{FV2E}	FRAME_VALID to EXPOSURE	[R0x06 -4] row-times - 21 SYSCLK-cycles (MIN)
t_{VBLANK}	Vertical blanking time	R0x06 row-times + 4 SYSCLK-cycles
t_{LEDOFF}	Required time between successive exposures (not shown in *Figure32*)	2 row-times + 4 SYSCLK-cycles (MIN)

Notes:
1. See “Row-Time Definition” on TN0960 for the row-time unit definition.
2. SYSCLK-cycle unit is defined as the reciprocal of the SYSCLK input frequency.
3. To change exposure time, change the total shutter width register (R0x0B).
4. To change frame rate, change the t_{E2E} value

The following registers must be configured to activate the snapshot mode:

Register	Name	Bit	Bit Name	Bit Description	Value
0x07	Chip control	3	Sensor master / slave mode	0 = slave mode 1 = master mode	1
0x07	Chip control	4	Sensor snapshot mode	0 = snapshot disabled 1 = snapshot mode enabled	1
0x07	Chip control	5	Stereoscopy mode	0 = stereoscopy disabled 1 = stereoscopy enabled	0
0x07	Chip control	6	Stereoscopic master / slave mode	0 = stereoscopic master 1 = stereoscopic slave	0
0x07	Chip control	8	Simultaneous / sequential mode	0 = sequential mode 1 = simultaneous mode	1
0x20	Reserved	2	CR enable	0 = normal operation 1 = CR enabled	1
0x20	Reserved	9	RST enable	0 = normal operation 1 = RST enabled	1
0xAF	AGC/AEC enable	0	AEC enable	0 = disable AEC 1 = enable AEC	0

Table 19: VM-010 Configuration Snapshot-Mode

The functions “automatic black level correction” and “automatic gain correction” are optimized for continuous capture modes. In snapshot mode, these functions should be set to manual mode (*black-level* register 0x47 bit 0 = “1”, *gain* register 0xAF bit 1 = “0”)

The Linux camera drivers from PHYTEC feature the selection between snapshot and master mode (default) from driver version V2.6.31.

Due to the structure of the *GStreamer* framework, the samples provided for GStreamer are not compatible with the snapshot mode.

Please refer to the sensor datasheet for more information.

4.5.5.2.2 Configurations of the Trigger Input

The CAM_TRIG signal is tied to low by a 4.7 kΩ resistor on the camera module. To release a trigger pulse, the signal must be driven to high state, V_{CAM} (3.3V). CAM_TRIG is available at the connectors listed below:

(a) at connector X101

The EXPOSURE signal (CAM_TRIG) can be routed to the CAM_CTRL2 pin (pin 30, X101) of the FFC connector. In default configuration, CAM_CTRL2 is tied to ground (GND). If CAM_CTRL2 is intended to be used as the trigger input, jumper J103 on the camera module is to be set to 2-3 position:

Signal	Pin	Function	I/O	Configuration
CAM_CTRL2	30	**GND**	-	**J107: 2-4**
		Trigger Input	I	J107: 2-3

Important note:

The CAM_TRIG function is an input signal. Before connecting the camera, please ensure that the corresponding Carrier Board or target hardware application board supports this function and is properly configured.

On PHYTEC Carrier Boards, *CAM_CTRL2* is connected to GND by default. Confirm the configuration options before connecting the *EXPOSURE* signals via X101 on the phyCAM board.

(b) at the connector X107

The *CAM_TRIG* signal is also available at the connector X107. This allows the connection of external trigger sources directly to the camera module.

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	LED_OUT / STROBE

Table 20: VM-010 X107 Connector

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

Note: We recommend using only one trigger input connection option at a time.

4.5.5.3 Strobe / LED-OUT

The *Strobe / LED-OUT* output indicates the period of time when the sensor is undergoing exposure. When exposure is active, this output is active high.

The signal is active during the complete period of sensor exposure (exposure time). This is the period of time the sensor is sensitive to light. Depending on whether the current exposure time is greater or less than the required readout time of the frame, there are two slightly different timing patterns (Figure54).

Note that the data can be read only in the following frame. Exposure and readout of a specific frame are thus in different frames.

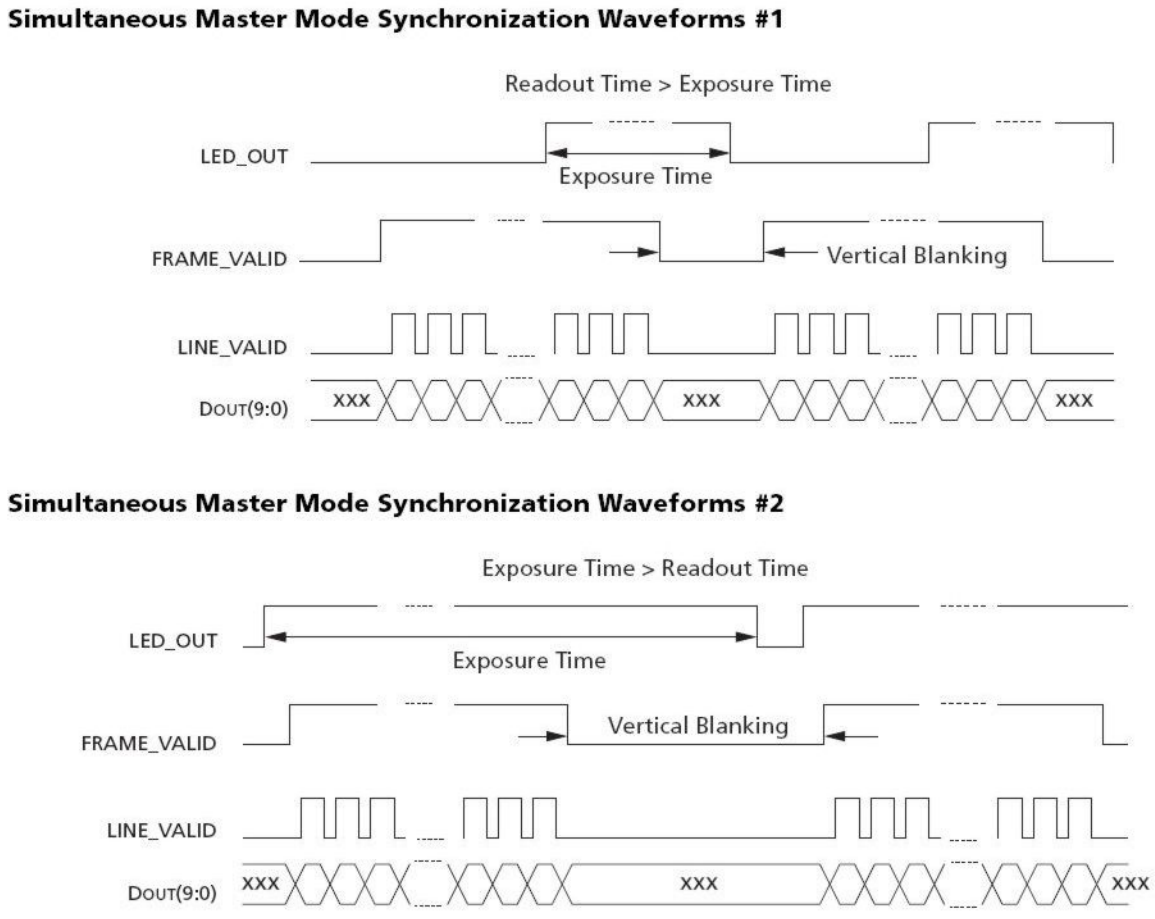


Figure54: VM-010 Timing Strobe/LED-OUT

The signal is available at the following connectors:

- *CAM_CTRL1* - pin 7 of the phyCAM-P connector (optional, depending on the configuration of the camera module)
- Pin 3 of the extension connector X107

4.5.5.3.1 Configuration of the Strobe Signal

The *LED_OUT* signal can be activated in the sensor register 0x1B. Furthermore, the polarity of the signal can be set as follows:

Register, 0x1B, LED_OUT		
Bit 0	Disable LED_OUT	Disable LED_OUT output. When cleared, the output pin LED_OUT is pulsed high when the sensor is undergoing exposure
Bit1	Invert LED_OUT	Invert polarity of LED_OUT output. When set, the output pin LED_OUT is pulsed low when the sensor is undergoing exposure

The Linux camera drivers provided by PHYTEC activate the *LED_OUT* signal by default in high-active state. Please refer to the datasheet of the camera sensor for more information about the *LED_OUT* signal.

4.5.5.3.2 Control of external light sources

The *Strobe/LED_OUT* signal is available at the connectors listed below:

(a) at connector X101 (phyCAM-P)
The phyCAM-P interface features multipurpose pins that can be configured for different features. The phyCAM-P can be configured in a way that *Strobe/LED_OUT* is routed to the *CAM_CTRL1* pin (pin 7, X101 of the FFC connector). In the default configuration *CAM_CTRL1* is routed to the *CAM_ADR0* signal. If CAM_CTRL1 is intended to be used as Strobe/LED_OUT, the following jumpers must be set:

- J102 to 1-2 position
- J103 must be closed

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	**I²C-Adress-Select**	I	**J102:2-4, J103:NOMT**
		Strobe Output	O	J102:1-2 or 2-3, J103:0R

Important Note:
The *Strobe/LED_OUT* signal is an output signal. Before connecting the camera, please ensure that the corresponding Carrier Board or target hardware application board supports this function and is configured properly. The *CAM_CTRL1* pin of must be configured as an input. Otherwise, the camera module might be damaged when connected.

CAM_CTRL1 of PHYTEC Carrier Boards is connected to GND by default. Therefore camera modules that are configured so that *LED_OUT* is routed to *CAM_CTRL1* may **not** be connected to a standard PHYTEC Carrier Board.

(b) at the connector X107
The LED_OUT signal is also available at the connector X107. This allows the connection of gated light sources directly to the camera module.

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	LED_OUT / STROBE

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

Note: We recommend using only one connection option at a time.

4.5.5.4 Reset

Applying a low-level (GND) at the reset input initiates a reset of the camera sensor. All registers are set to their default values. The reset input should be connected to the /RESET output of the microcontroller board. The reset signal must be held on high-level during operation of the camera module.

4.5.5.5 Standby-Mode

CAM_CTRL2 can be configured to act as a an input to control the camera sensor's standby signal:

Signal	Pin	Function	I/O	Configuration
CAM_CTRL2	30	Standby	I	J107:1-2

The sensor goes into standby mode by setting STANDBY to HIGH. Once the sensor detects that STANDBY is asserted, it completes the current frame before disabling the digital logic, internal clocks, and analog power enable signal. To release the sensor out from the standby mode, reset STANDBY back to LOW. See the sensor's datatsheet for more information on standby mode.

4.5.5.6 Output-Enable

The output-enable input allows control of the data lines CAM_DD[0...9]. Applying a high-level to this input will tristate these outputs. For normal operation, output enable must be at low-level (GND).

4.5.6 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

4.6 VM-011 – phyCAM-P camera module

5 MPixels – monochrome /color

4.6.1 Specification

Features

- 5 MPixels – sensor (5,038,848 pixels)
- monochrome (VM-011-BW) or color (VM-011-COL)
- phyCAM-P – interface
- Framerate 15 fps at full resolution
- Framerate 60 fps at HD 720p
- Rolling Shutter
- External Trigger and Strobe
- Secondary connector with trigger and strobe (optional)

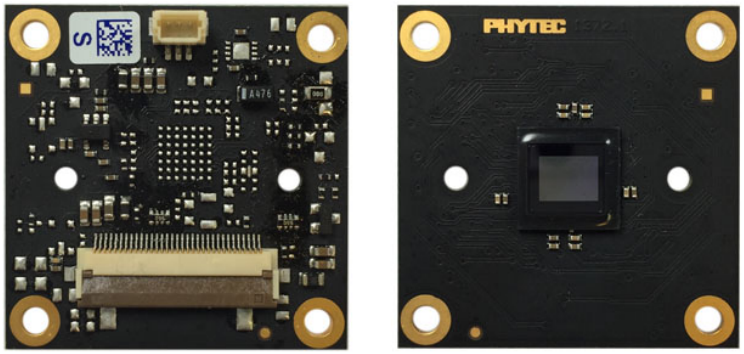


Figure55: VM-011 (phyCAM-P, PL1372.1) (rear / front view)

Parameters

	VM-011-BW	VM-011-COL
Sensor		
Resolution	5 Megapixels	5 Megapixels
Pixels (H x V)	2592 x 1944	2592 x 1944
Sensor Size	1/2.5" 5.7 mm x 4.28 mm	1/2.5" 5.7 mm x 4.28 mm
Pixel Size	2.2 µm x 2.2 µm	2.2 µm x 2.2 µm
Color / Monochrome	monochrome	color
Technology	CMOS	CMOS
Image Sensor	Aptina MT9P031	Aptina MT9P006
Scan System	progressive	progressive
Shutter Type	rolling	rolling
Fame rate (fps)	15 fps at full resolution	15 fps at full resolution
	60 fps at HD 720p	60 fps at HD 720p
Video Resolution	n/a	n/a
Responsivity	1.4 V/lux-sec	1.76 V/lux-sec
Max. Dynamic Range	70.1 dB	67.74 dB
High Dynamic Range	n/a	n/a
Exposure Time	programmable	programmable
Gain	programmable	programmable
AEC	n/a	n/a
AGC	n/a	n/a
Gamma Correction	n/a	n/a
White Balance/AWB	n/a	manual
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	ja	ja
Skipping	2x2 / 3x3	2x2 / 3x3
Binning	2x2 / 4x4	2x2 / 4x4
Mirror	programmable	programmable
Image Processor	n/a	n/a
LED-Light	n/a	n/a
Special features	see section 4.6.5	see section 4.6.5

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-P	phyCAM-P
Data Format	8 / 10 Bit parallel	8 / 10 Bit parallel
Interface-Mode	Y8 / Y10	8/10 Bit RGGB (Bayer)
Dataline-Shifting	n/a	n/a
Camera Config. Bus	I²C	I²C
Supply Voltage	2.8 V	2.8 V
Power Consumption	450 mW	450 mW
Pwr. Consumpt. Standby	2 mW	2 mW

Mechanical Parameters		
Lens Connector	without / M12 / C-CS	without / M12 / C-CS
Lens	n/a	n/a
Housing	n/a	n/a
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	n/a	n/a
Weight (PCB)	5 g	5 g
Operating Temperature	-25...70°C	-25...70°C

Connectors		
Data and Power	FFC 33 pin	FFC 33 pin
Trigger / Sync.	FFC + JST 3-pin	FFC / JST 3-pin
Iris	n/a	n/a
Special functions	n/a	n/a

n/a: not applicable. All parameters are subject to change

Table 21: Parameters VM-011 (phyCAM-P)

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	2,6	2,8	3,1	V
Operation Current	I_{CAM}	tbd	202	tbd	mA
Input high voltage[1]	V_{IH}	2.1	2.8	-	V
Input low voltage[1]	V_{IL}	-	0	0.7	V
Input high voltage[2]	$V_{IHTrigger}$	2	2.8	3.3	V
Input low voltage[2]	$V_{ILTrigger}$	-	0	0,8	V
Output high voltage[3]	V_{OH}	2.2	-	-	V
Output low voltage[3]	V_{OL}	-	-	0.5	V
Output high voltage[4]	$V_{OHStrobe}$	1.9	2.8	-	V
Output low voltage[4]	$V_{OLStrobe}$	-	0.16	0.4	V
Voltage Set Resistor	R_{31}	215	220	224	Ω
Operating Temperature[5]	T_{OP}	-25	-	70	°C
Storage Temperature[5]	T_{STG}	-25	-	70	°C

[1] CAM_SDA, CAM_SCL, CAM_MCLK, CAM_CTRL1, CAM_CTRL2, CAM_RST and CAM_OE
[2] CAM_TRIGGER
[3] I=±100µA / CAM_DD0 to CAM_DD9, CAM_FV, CAM_LV, CAM_SDA and CAM_SCL
[4] CAM_STROBE
[5] -30°C without the optional Trigger/Strobe-connector X2

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	6	-	96	MHz
Clock Duty Cycle	$dutycyle_{MCLK}$	40	50	60	%
MCLK to PCLK delay	t_{CP}	11.5	17.7	19.1	ns
PCLK to data valid	t_{PD}	0.8	2.1	3.9	ns
PCLK to FV high	t_{PFH}	2.8	4.3	5.9	ns
PCLK to FV low	t_{PFL}	2.4	4.2	5.9	ns
PCLK to LV high	t_{PLH}	2.2	3.5	5.9	ns
PCLK to LV low	t_{PLL}	2.6	4.1	5.9	ns
I²C Frequency	f_{I2C}	-	100	400	kHz

Data Formats

Monochrome (VM-011-BW):

- Y8 : 8 bit grey scale
- Y10: 10 bit grey scale

Color (VM-011-COL):

- RGGB (Bayer-Pattern) up to 10 bit color depth

Notes

- Any other desired lower color / grey scale resolution can be configured by using a reduced subset of the data lines. To configure this, connect only the upper data lines (MSB) to the microprocessor interface. Some microprocessors also enable dynamic configuration of the camera interface input.

Spectral Characteristics

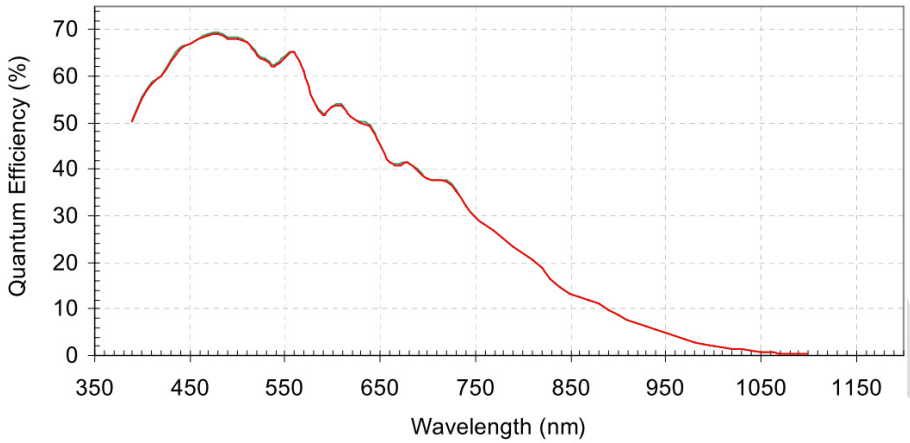


Figure56: Spectral Characteristics VM-011-BW

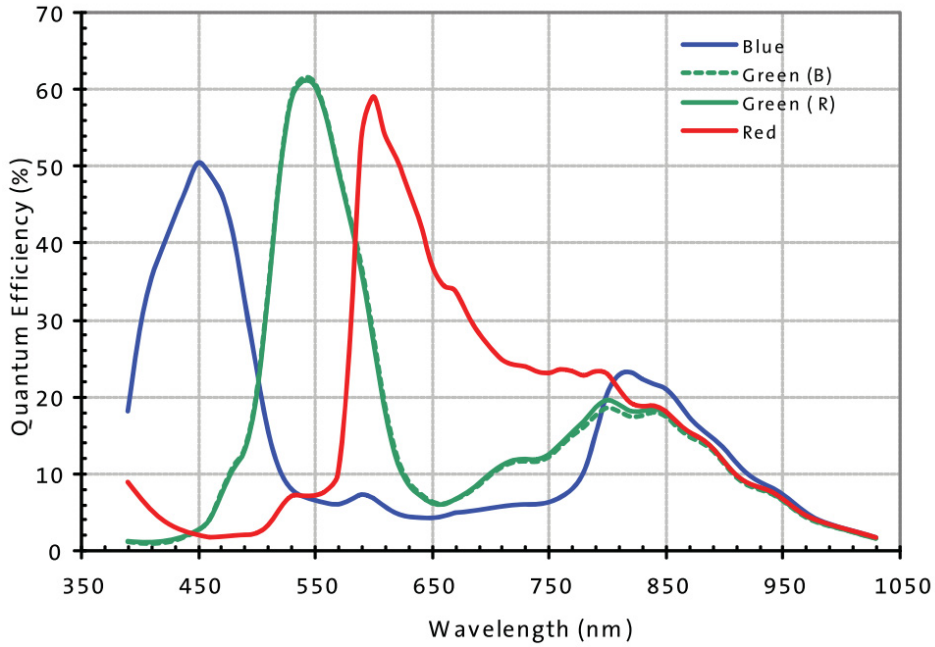


Figure57: Spectral Characteristics VM-011-COL

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

4.6.2 I²C Addresses

Device	I²C-Address	Configuration		Variant
		CAM_CTRL1	J11	
Camera Sensor	0x90	x	2+3	all
		GND	**2+4**	
	0xBA	x	1+2	
		V_{CAM}	**2+4**	

Device	I²C-Address	Configuration			Variant
		J13	**J14**	**J15**	
EEPROM	0xA0	1+2	1+2	1+2	all
	0xA2	2+3	1+2	1+2	
	0xA4	1+2	2+3	1+2	
	0xA6	2+3	2+3	1+2	
	0xA8	1+2	1+2	2+3	
	0xAA	2+3	1+2	2+3	
	0xAC	1+2	2+3	2+3	
	0xAE	**2+3**	**2+3**	**2+3**	

Default configuration of the camera sensor (printed bold):
0x90 (CAM_CTRL1 = low)

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

4.6.3 Feature Pins

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	N.C. (not connected)	-	J8:NOMT, J11:not 2+4
		I²C-Adress-Select	**I**	**J8:NOMT, J11:4+2**
		Strobe Output	O	J8:1+2, J11: not 2+4
		CAM_D0	O	J8:2+3, J11: not 2+4
CAM_CTRL2	30	**GND**	**-**	**J3:NOMT, J4:1+2**
		Trigger Input	I	J3:2+3, J4:NOMT
		/Standby	I	J3:1+2, J4:NOMT
		N.C. (not connected)	-	J3:NOMT, J4:NOMT
		CAM_D1	O	J3:NOMT, J4:2+3
CAM_RST	3	/Camera Reset	I	active low
CAM_OE	32	**N.C. (not connected**	**-**	**J6:1+2**
		Data Output Enable	I	J6:2+3
CAM_MCLK	29	**Master Clock**	**I**	**J16:2+3 (22Ω)**
		N.C. (not connected)	-	J16:1+2 (22Ω)

Notes:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

“not x+y” = Jumper must be set to a different setting.

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

4.6.4 Jumper Map VM-011

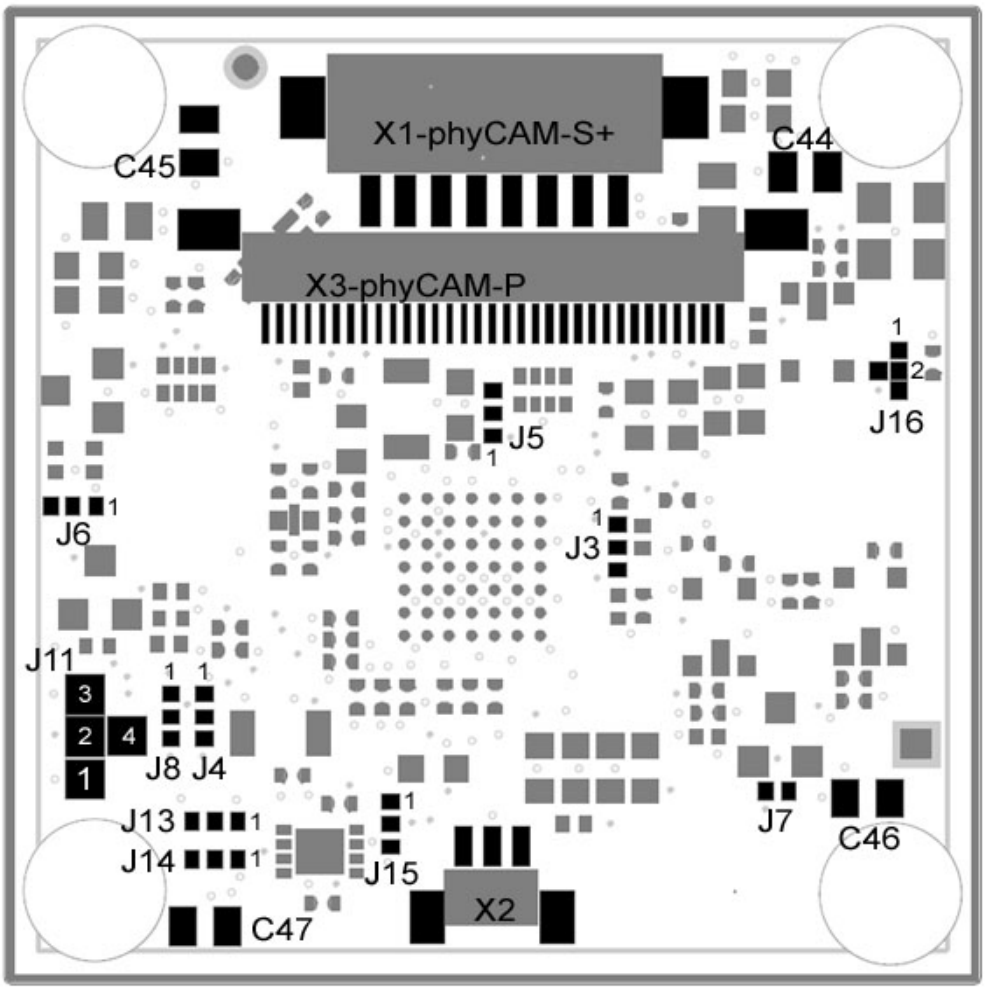


Figure58: Jumper Map VM-011, PL1372.1

4.6.5 Special Features VM-011

4.6.5.1 Variable Resolution

As with other members of the phyCAM product family, the image resolution of the VM-011 module can be reduced virtually. This allows the user to adapt the captured image size and the amount of data sent to the microcontroller to the needs of the appliocation. Reducing the image resolution can also result in a higher framerate. The following table shows some examples for typical sub-resolutions for the VM-011 camera module:

	Resolution options			
Image Resolution	Name	max. Frame rate	Mode	Format
2592 x 1944	-	15	window	1/2.5"
2048 x 1536	QXGA	21	window	1/3"
1920 x 1080	FullHD	31	window	1/3"
1600 x 1200	UXGA	31	window	1/4"
1280 x 1024	SXGA	42	window	1/4.5"
1280 x 720	HD	60	binning	1/2.5"
1024 x 768	XGA	63	window	1/5.5"
		63	skipping	1/3"
		47	binning	1/3"
800 x 600	SVGA	90	window	1/6"
		90	skipping	1/4"
		65	binning	1/4"
640 x 480	VGA	123	window	1/6.5"
		123	skipping	1/2.5"
		53	binning	1/2.5"

Depending on the application's requriements different modes can be used to reduce the resolution:

- *window:*
  Only a part of the physical image sensor is used (*Region of Interest* – ROI). Pixels outside this window are skipped. This mode reduces the effective size of the image sensor. This must be taken into consideration when calculating the lens parameters for the system.

The start position of the ROI window can be moved on the physical image sensor field which allows electronical panning.

- *binning:*
  Binning combines adjacent pixels on the sensor. The effective pixel size is higher that the size of a single pixel. By this, the light sensitivity of the sensor is increased.
  For color sensors not the direct neighbor pixels are combined but the next pixels with the same color filter (see the datasheet of the sensor for details).
- *skipping:*
  During readout pixels in the image field are skipped. This reduces the image resolution but has hardly any impact on the effective sensor size. This can be helpful for lens selection or if switching between different modes is desired (electronical zoom).
  Compared to binning, skipping allows higher framerates.

4.6.5.2 Trigger / Bulb Exposure

This input allows precise control of the point in time an image is captured or the exposure time by an electrical signal:

- In Snapshot-Mode, this input controls the point in time an image is captured by the sensor. A low-level at the trigger input initiates an image capture.
- In Bulb Exposure-Mode the exposure time is controlled by this input..

More information about these modes can be found in the sensor datasheet.

The trigger input is available at the pin *CAM_CTRL2* of the phyCAM-P connector (J3 has to be set to 2-3 and J4 must be open).
This trigger input is also available at pin 1 of the extension connector X2.

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	STROBE

Table 22: VM-011 X2 Connector

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

Note
Polarity of the signal can be changed by programming the sensor's register.

4.6.5.3 Strobe

The *Strobe* output indicates the period of time when the sensor is undergoing exposure. When exposure is active, this output is active high.

More information about the strobe signal configuration can be found in the datasheet of the image sensor.

The signal is available at the following connectors:

- *CAM_CTRL1* - pin 7 of the phyCAM-P connector (optional, depending on the configuration of the camera module)
- Pin 3 of the extension connector X2

4.6.5.4 Reset

Applying a low-level (GND) at the reset input initiates a reset of the camera sensor. All registers are set to their default values. The reset input should be connected to the /RESET output of the microcontroller board. Ensure that the /RESET signal is asserted during power up of the sensor The reset signal must be held on high-level during operation of the camera module..

4.6.5.5 Output-Enable

The output-enable input (*CAM_OE* , pin 32 of the phyCAM-P connector) allows control of the data lines CAM_DD[0...9], the sync signals CAM_LV, CAM_FV, CAM_PCLK and the STROBE signal. Applying a high-level to this input will tristate these outputs. For normal operation, output enable must be at low-level (GND).

This function is enabled by setting jumper J6 to 2+3 position. The default configuratiom is J6=1+2 which permanently enables the outputs regardless of the state of the *CAM_OE* input.

4.6.5.6 I²C-EEPROM

As an option, a serial I²C EEPROM can be installed on the VM-011 camear module. The EEPROM can be used to store application data such as calibration data.
The EEPROM type is M24C02-RMC6TG. It features a size of 2 kBit.
The default I^2C-address of the EEPROM is 0xAE.
Other addresses can be selected by setting J13, J14 and J15 (see section 5.6.2).
Data transfer rate: 100 kHz Standard Mode / 400 kHz Fast Mode

For more information please refer to the EEPROM's datasheet.

4.6.5.7 12 Bit Data Interface

Despite the camera sensor features a 12 bit wide data interface, only 10 bit, CAM_D[11..2], are available on the phyCAM-P connector:

Assignment of data lines:

Image Data Out	Sensor Interface
CAM_CTRL1*	D0
CAM_CTRL2*	D1
CAM_DD0	D2
CAM_DD1	D3
CAM_DD2	D4
CAM_DD3	D5
CAM_DD4	D6
CAM_DD5	D7
CAM_DD6	D8
CAM_DD7	D9
CAM_DD8	D10
CAM_DD9	D11

*) only if activated by jumper setting

As an option, the two lowest data bit D0 and D1 can be routed to the *CAM_CTRL1* and *CAM_CTRL2* pins of the phyCAM-P connector. See the table in section 4.6.3 to determine the corresponding jumper settings (J3, J4, J8 and J11).

4.6.5.8 Internal MCLK Oscillator

As an option, the camera board can be populated with a crystal oscillator. This allows the generation of the master clock MCLK on board so no external MCLK clock has to be fed into the board on pin 29 of the phyCAM-P connector.
For using the internal clock source, XT1 has to be populated and J1 must be set to 1+2 position.

4.6.6 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

4.7 VM-012 – phyCAM-P
1.3 MPixels Global Shutter – monochrome /color

4.7.1 Specification

Features

- 1.3 MPixels – sensor (1,310,720 pixels)
- monochrome (VM-012-BW) or color (VM-012-COL)
- phyCAM-P – interface
- Framerate: 37 fps at full resolution
- Framerate: 130 fps at VGA resolution
- Global Shutter and Rolling Shutter (selectable)
- Externer Trigger and Strobe
- Secondary connector with trigger and strobe (optional)

Figure59: VM-012 (phyCAM-P) (front / rear view)

Parameters

	VM-012-BW	VM-012-COL
Sensor		
Resolution	1,3 MPixels	1,3 MPixels
Pixels (H x V)	1280 x 1024	1280 x 1024
Sensor Size	1/2" 6.18 mm x 4.95 mm	1/2" 6.18 mm x 4.95 mm
Pixel Size	4.8 µm x 4.8 µm	4.8 µm x 4.8 µm
Color / Monochrome	monochrome	color
Technology	CMOS	CMOS
Image Sensor	ON Semiconductor VITA 1300 (NOIV2SN1300A-QDC)	ON Semiconductor VITA 1300 (NOIV2SE1300A-QDC)
Scan System	progressive	progressive
Shutter Type	global or rolling	global or rolling
Fame rate (fps)	37 fps (full resolution) 130 fps at VGA	37 fps (full resolution) 130 fps at VGA
Responsivity	4.6 V/lux·sec (at 550 nm)	4.6 V/lux·sec (at 550 nm)
Max. Dynamic Range	60 dB (Rolling Shutter Mode) 53 dB (Global Shutter Mode)	60 dB (Rolling Shutter Mode) 53 dB (Global Shutter Mode)
High Dynamic Range	90 dB	90 dB
Exposure Time	programmable	programmable
Gain	programmable	programmable
AEC	automatic and manual	automatic and manual
AGC	automatic and manual	automatic and manual
Gamma Correction	n/a	n/a
White Balance/AWB	n/a	n/a
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	up to 8	up to 8
Skipping	2x2	2x2
Binning	2x2	2x2
Mirror	n/a	n/a
Image Processor	n/a	n/a
LED-Light	n/a	n/a
Special features	see section 4.7.7	see section 4.7.7

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-P	phyCAM-P
Data Format	8 / 10 Bit parallel	8 / 10 Bit parallel
Interface-Mode	Y8 / Y10	8 / 10 Bit RGGB (Bayer)
Dataline-Shifting	n/a	n/a
Camera Config. Bus	I²C	I²C
Supply Voltage	3.3 V	3.3 V
Power Consumption	450 mW	450 mW
Standby Power	26 mW	26 mW

Mechanical Parameters		
Lens Connector	without / M12 / C-CS	without / M12 / C-CS
Lens	n/a	n/a
Housing	n/a	n/a
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	n/a	n/a
Weight (PCB)	5 g	5 g
Operating Temperature	-25...85°C	-25...85°C

Connectors		
Data and Power	FFC 33 pin	FFC 33 pin
Trigger / Sync.	FFC + JST 3 pin	FFC / JST 3 pin
Iris	n/a	n/a
Special functions	n/a	n/a

n/a: not applicable. All parameters are subject to change

Table 23: Parameters VM-012 (phyCAM-P)

Electrical Specifications

	Symbol	min.	typ.	max.	Unit
Operating Voltage	V_{CAM}	3.1	3.3	3.6	V
Operation Current	I_{CAM}	tbd	450	tbd	mA
Input high voltage	V_{IH}	2	-	V_{CAM} +0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Output high voltage	V_{OH}	2,4	-	-	V
Output low voltage	V_{OL}	-	-	0.5	V
Voltage Set Resistor	R_{31}	-	0	2	Ω
Operating Temperature [1]	T_{OP}	-25	-	85	°C
StorageTemperature [1]	T_{STG}	-25	-	85	°C

[1] -30°C without the optional Trigger/Strobe-connector

	Symbol	min.	typ.	max.	Unit
Master Clock Frequency	f_{MCLK}	20	-	62	MHz
Clock Duty Cycle	$dutycyle_{MCLK}$	40	50	60	%
Input Clock jitter	tj	-	20	-	ps
MCLCK to PCLK delay	t_{CP}		tbd.		ns
PCLK to data valid	t_{PD}		tbd.		ns
PCLK to FV high	t_{PFH}		tbd.		ns
PCLK to FV low	t_{PFL}		tbd.		ns
PCLK to LV high	t_{PLH}		tbd.		ns
PCLK to LV low	t_{PLL}		tbd.		ns
I²C Frequency[2]	f_{I2C}	-	100	400	kHz

[2] the I²C master must support Clock-Stretching

Data Formats

Monochrome (VM-012-BW):

- Y8 : 8 bit grey scale
- Y10: 10 bit grey scale

Color (VM-012-COL):

- RGGB (Bayer-Pattern) 8 bit color depth
- RGGB (Bayer-Pattern) 10 bit color depth

Notes

- Any other desired lower color / grey scale resolution can be configured by using a reduced subset of the data lines. To configure this, connect only the upper data lines (MSB) to the microprocessor interface. Some microprocessors also enable dynamic configuration of the camera interface input.

Spectral Characteristics

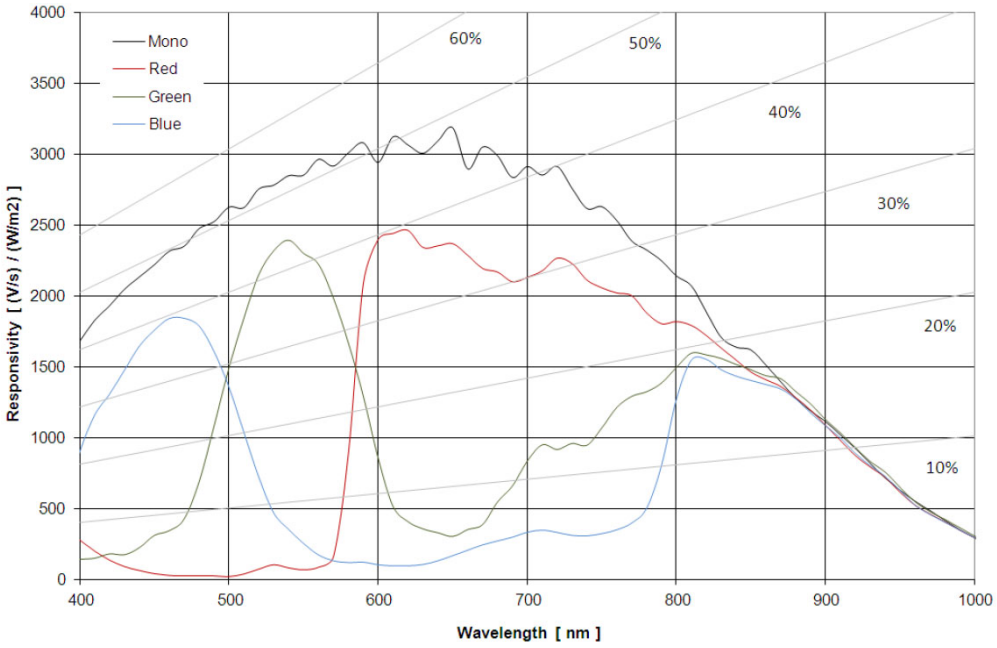


Figure60: Spectral Characteristics VM-012-BW / COL

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

4.7.2 I²C Addresses

Device	I²C-Address	Configuration				
		CAM_CTRL1	J11	J9	J10	Variant
Camera Sensor	**0x90**	**GND**	**1-2**	**2-4**	**1-2**	all
		x	x	2-3		
	0x98	V_{CAM}	**1-2**	**2-4**	**1-2**	
		x	x	1-2		
	0xB0	GND	1-2	2-4	2-3	
		x	x	2-3		
	0xB8	V_{CAM}	1-2	2-4	2-3	
		x	x	1-2		

Device	²C-Address	Configuration n			Variant
		J2	J3	J4	
EEPROM	0xA0	1+2	1+2	1+2	optional
	0xA2	2+3	1+2	1+2	
	0xA4	1+2	2+3	1+2	
	0xA6	2+3	2+3	1+2	
	0xA8	1+2	1+2	2+3	
	0xAA	2+3	1+2	2+3	
	0xAC	1+2	2+3	2+3	
	0xAE	**2+3**	**2+3**	**2+3**	

Default configuration of the camera sensor (printed bold):
0x90 (CAM_CTRL1 = low)

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

4.7.3 Feature Pins

Signal	Pin	Function	I/O	Configuration
CAM_CTRL1	7	N.C. (not connected)	-	J11:NOMT
		I²C-Adress-Select	**I**	**J11:1+2**
		Monitor Out	O	J11:2+3
CAM_CTRL2	30	**GND**	**-**	**J5:1+2**
		Trigger Input	I	J5:2+3
		N.C. (not connected)	-	J53:NOMT
CAM_RST	3	**/Camera Reset**	**I**	**aktiv low**
CAM_OE	32	reserved	**-**	default: input without function
CAM_MCLK	29	**Master Clock**	**I**	**J1:2+3**
		N.C. (not connected)	-	J1:1+2

Notes:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

“not x+y” = Jumper must be set to a different setting.

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

4.7.4 Jumper Map VM-012

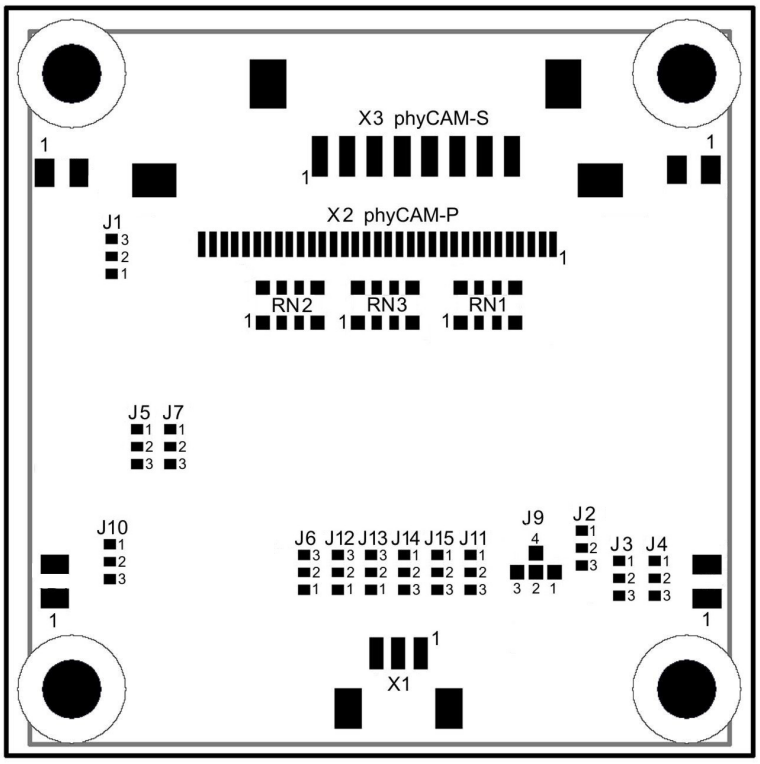


Figure61: Jumper Map VM-012, PL1420.0

4.7.5 Pixel Remapping VM-012

The pixels of the VITA 1300 image sensor are organized in kernels. This means that the readout sequence of the pixels in a line is not sequentially consecutive as one would assume from the physical position of the pixel on the sensor.
The kernel size is 8 pixels in x-direction by 1 pixel in y-direction. Figure62 indicates how the kernels are organized.

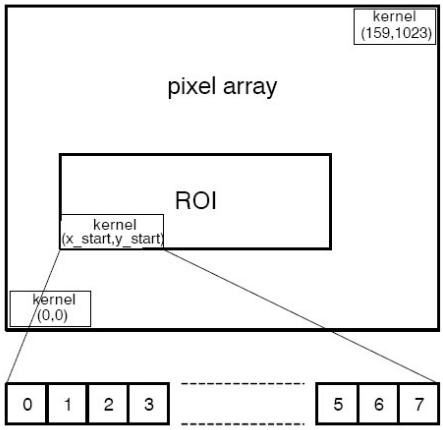


Figure62: Kernel organization in pixel array (VM-012)

The data order of the image data on the output channels depends on the subsampling mode:

(a) no subsampling

The pixel sequence is different for even and odd kernels like shown in Figure63:

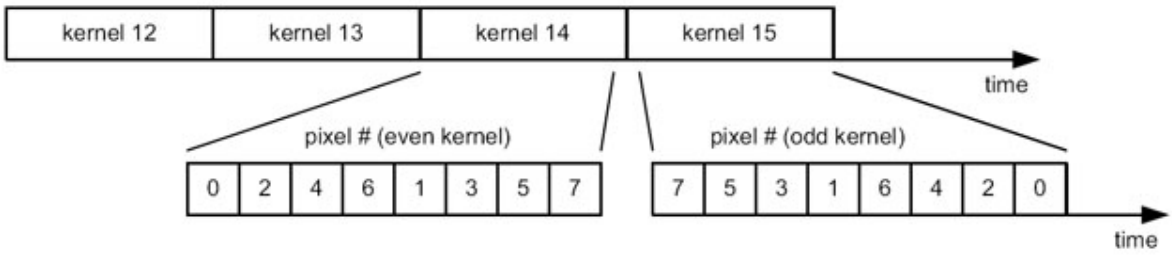


Figure63: Pixel order with no subsampling (VM-012)

(b) subsampling, monochrome sensor

In subsampling mode two adjacent kernels are combined to one single kernel (see figure below). By this the number of pixels are reduced by two. Only the pixels at the even pixel positions inside that kernel are read out. Figure64 shows the data order.
Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no-subsampling’ readout.

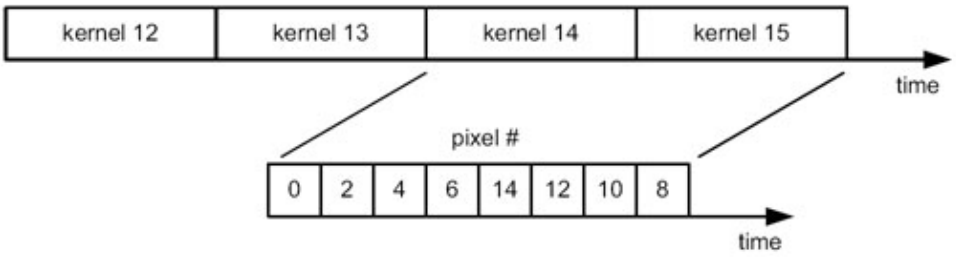


Figure64: Pixel order with subsampling, monochrome sensor

(c) subsampling, color sensor

In subsampling mode two adjacent kernels are combined to one single kernel (see figure below). By this the number of pixels are reduced by two. Only the pixels 0, 1, 4, 5, 8, 9, 12, and 13 are read out. Figure75 shows the data order.
Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no-subsampling’
readout.

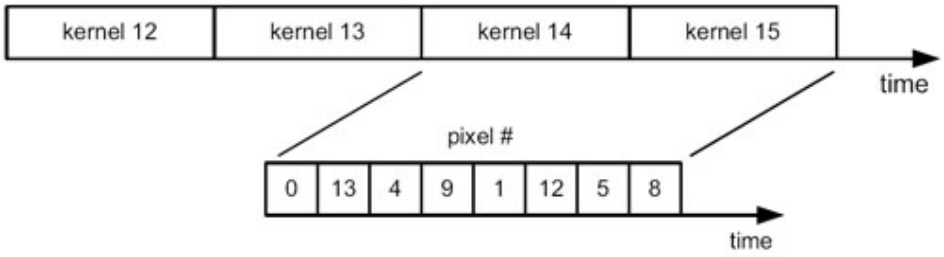


Figure65: Pixel order with subsampling, color sensor

Notes
The following processing unit must re-order the pixel seqence (for example by software) or the pixel order described above must be taken into consideration when processing the image data.

If ROIs are defined the borders of the ROI window must meet the borders of the kernels. Ideally the beginning of the ROI window is aligned in a way that it meets the same kernel type (even kernels).

Note
With the development kits Phytec ships a library and a GStreamer-function for pixel remapping.
See the Application Note „VM-012 Remapping“ for more details.

4.7.6 I²C Interface VM-012

For communication with the components on the camera module (like image sensor, EEPROM, etc.) the phyCAM interface features an I²C interface. I²C communication is used for phyCAM-P and phyCAM-S(+) also.
Via the I²C interface the CPU can read and write the registers of the camera sensor. By that the configuration of the sensor can be set.
In contrast to the phyCAM interface the VITA 1300 sensor uses a SPI interface for sensor control. On the VM-012 camera an additional microcontroller is used to translate the I²C bus of the phyCAM interface to SPI. This allows the VM-012 to be compatible to the phyCAM-P and phyCAM-S+ standard.
Because of the bus translation some particularites in I²C communication have to be considered.

The I²C interface of the VM-012 is organized in 8-bit data blocks:

- 8-Bit device address
- 8-Bit register address
- 2 x 8-Bit data

I²C access is always carried out by a 16-bit write or 16-bit read protocol.

According to the I²C specification the selection between read and write access is determined by the LSB of the device address.

- write access: LSB of the device address = 0
- read access: LSB of the device address = 1

4.7.6.1 16-Bit Write Sequence

Figure66 shows a typical sequence for writing a value into a 16 bit register. The master initiates the sequence by a start bit, followed by the register address and two data bytes. The byte order is most significant byte first.
After each byte an acknowledge (ACK) is sent by the VM-012. After the transmission of all 16 data bits the register content is updated. The master finishes the write cycle by sending a stop bit.

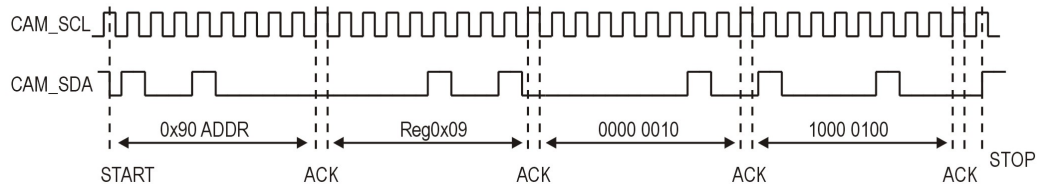


Figure66: Writing the value 0x0284 into register 0x09 of device 0x90

Note
The data transmitted by the I²C write cycle are written into the register of the camera sensor after the write cycle is completed.
For that, an internal SPI bus cycle is executed.

Before a new I²C access is initiated the master has to wait until the internal SPI bus cycle ic completed.
To ensure this, one of the two methods described below can used:

Method 1:
After an I²C write access the master waits a given time before he starts the next I²C access to the camera. With firmware version V0.4 of the VM-012 the minimum waiting period time after the end of an I²C write access to the camera is 250µs.

Method 2:
The status flag *SPI_WRITE* in the register *VM012_STATUS* (0x99) can be used to determine the end of the internal write cycle.
This status flag is controlled by the internal microcontroller of the camera module..
The bit is set after a write command is detected. It is reset after the completion of the internal write cycle.
The status register is described in the next section.

Note
The registers VM012-STATUS, VM012-CONTROL and VM012_FIRMWARE can be accessed any time without any waiting period. Especially this registers can be accessed while an interal write cycle is in progress.

4.7.6.2 16-Bit Read Sequence

A typical 16-bit read sequence is shown in Figure67. First the master has to write the register address, as in a write sequence. Then a start bit and the device address with LSB set specifies that a read is about to happen from the register. Note that the LSB set in the device address indicates read access.
With the following clocks the camera module outputs two data bytes which contain the 16 bit register content, high-byte first. After each 8 bit width Byte the master sends an acknowledge bit (ACK). The data transfer is finished by the master by sending a No-Acknowledge-Bit (NACK) after 16 bits of data have been transferred.

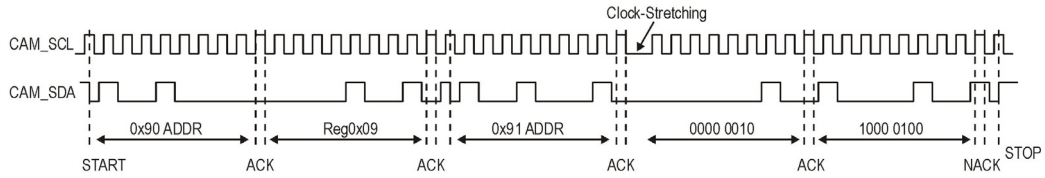


Figure67: Reading the value 0x0284 from register 0x09 of device 0x90

Note:
No waiting time is needed after the initial write command of a read sequence. The following read command can be sent immediately.

After the internal microcontroller of the VM-012 has received the internal I²C write command and the device address with read bit set, it takes approx. 200µs to process the command internally. The master of the I²C has to wait this time before he can start reading the data from the camera module.
For this the VM-012 uses the „*Clock-Stretching*“ method. „*Clock-Stretching*“ is used only before the first data byte. The secons byte is transferred immediately.

Note:
The I²C-Master must support *Clock-Stretching*.

4.7.6.3 VM-012 Internal I²C Registers

4.7.6.3.1 Paging

The camera sensor VITA 1300 of the VM-012 has a register map with in total 511 registers. However many I²C routines support a register space of 255 registers only.
To allow easy access to all sensor registers by all systems, the VM-012 uses paging. By that the I²C-adress space is split into two pages of 255 registers. A page bit is used to select beteween lower and higher address space:

page bit	I²C-address sent to VM-012	acessed register of the VITA 1300 camera sensor
0	0x00 ... 0xFF	0x000 ... 0x0FF
1	0x00 ... 0xFF	0x100 ... 0x1FF

The sensor register accessed can be calculated by the following equation:

```
sensor_register = page_bit · 0x100 + I²C_register_address
```

The *PAGE_BIT* is located in the *VM012_CONTROL* register.

Note:
A description of the sensor's registers can be found in the VITA 1300 datasheet.

4.7.6.3.2 Control- and Status Registers

Note:
The following information refer to firmware version V0.5

Three additional registers are inserted into the register map of the camera sensor to control the internal microcontroller of the VM-012 and to read status informations.
Read and write accesses to this registers are processed by the microcontroller of the VM-012. These acesses are not passed to the VITA 1300 image sensor.
Because this three addresses are not uses by the VITA 1300, this does not interfere with any functions of the sensor.

VM-012 I²C Register Address	Page-Bit	Read	Description
0x97	x	R	Firmware-Version der VM-012
0x98	x	R/W	VM_012_CONTROL Register
0x99	x	R	VM_012_STATUS Register

x = don't care, R = read only, R/W = read and write access

Note:
This three registers are processed directly by the microcontroller of the VM-012. They are not transmitted via SPI to the image sensor. Therefore, no delay or waiting time is needed when accessing this registers..

Register description VM012_FIRMWARE; 0x97 (151 decimal)

0x97 – VM012_FIRMWARE					
Bit	**Bit Name**	**Bit Description**	**Default Hex (Dec)**	**Legal Values (Dec)**	**Read/ Write**
7...0	MINOR_REVISION	Firmware revision (minor part)	-	0...255	R
15...8	MAJOR_REVISION	Firmware revision (major part)	-	0...255	R

Register description VM012_CONTROL; 0x98 (152 decimal)

0x98 – VM012_CONTROL					
Bit	**Bit Name**	**Bit Description**	**Default Hex (Dec)**	**Legal Values (Dec)**	**Read/ Write**
0	PAGE_BIT	Page selection of the image sensor register: 0 = access registers 0x000 ... 0x0FF 1 = access registers 0x100 ... 0x1FF The page bit does not change its state after a camera reset.	0	0 ; 1	R/W
1	AUTO_SENSOR_RESET	Auto Software image sensor reset 0 = default state 1 = excecute camera sensor reset cycle Writing a 1 to this bit initiates an automatic reset cycle of the image sensor. The reset signal of the sesor is asserted and the sensor's power supply is switched off. After a delay of 100ms the sensor is powered up again and sensor reset is deasserted. This bit is reset automatically after the sensor reset cycle has finished.	0	0 ; 1	R/W
2	SENSOR_RESET	Image sensor reset 0 = default state 1 = image sensor reset Writing a 1 to this bit asserts the reset signal of the image sensor and the sensor's power supply is switched off. The image sensor is kept in this state until the bit is reset to 0. Resetting this bit to 0 will power up the sensor and deassert the sensor reset. This function can be used as a power saving state.	0	0 ; 1	R/W
3...7	RESERVED	reserved	-	-	-
8	VM-012_RESET	Camera module reset 0 = default state 1 = excecute camera module reset cycle Writing a 1 to this initiates a camera module reset cycle. A reset of the camera sensor and of the internal microcontroller is performed. After the reset cycle all registers are set to their default values.	0	0 ; 1	R/W
9...15	RESERVED	reserved	-	-	-

Register description VM012_STATUS; 0x99 (153 decimal)

0x99 – VM012_STATUS					
Bit	**Bit Name**	**Bit Description**	**Default Hex (Dec)**	**Legal Values (Dec)**	**Read/ Write**
0	SPI_READ	0 = SPI-READ idle 1 = SPI-READ in progress – only registers 0x97, 0x98 and 0x99 may be accessed. Note: If clock stretching is used, I²C read delay is inserted automatically. In this case it's not necessary to observe this status bit.	0	0 ; 1	R
1	SPI_WRITE	0 = SPI-WRITE idle 1 = SPI-WRITE in progress. While this bit is set, only registers 0x97, 0x98 und 0x99 may be accessed.	0	0 ; 1	R
2..15	RESERVED	reserved	-	-	-

4.7.7 Special Features VM-012

4.7.7.1 Windowing / ROI

As with other members of the phyCAM product family, the image resolution of the VM-012 module can be reduced virtually. This means that only the user-selected Regions Of Interest (ROI) are read out.
This allows the user to adapt the captured image size and the amount of data sent to the microcontroller to the needs of the appliocation. Reducing the image resolution can also result in a higher framerate.

Abhängig von der Betriebsart können mehrere ROIs definiert werden:

- In global shutter mode, up to eight ROIs can be configured.
- In rolling shutter mode, only a single ROI is supported.

Note that if multiple ROIs are active, the pixel output order is determined by the physical position of the corresponding pixel on the sensor. This means that ROIs are masking the sensor, but they do not change the output seqence of the pixel data. Depending on the position of the multiple ROIs, the active pixels of the ROIs are nested.

4.7.7.2 Trigger

The trigger input can be configured in two ways:

- Triggered Shutter Master Mode
  In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting.

- Pipelined Shutter Slave Mode
  In this mode, the start of the integration and the integration time is controlled by the trigger signal.
  Integration starts with a rising edge of the trigger signal and is ended with the falling edge.

Note:
Trigger may not be activated during the Frame Overhead Time (FOT). The signal *First Line Indication* can be used to detect the image start. *First Line Indication* is a configuration mode of the *Monitor* signal (see 4.7.7.3).
Details of the trigger function are described in the datasheet of the image sensor VITA 1300.

The trigger input is available on two connectors:

- On the CAM_CTRL2 - pin of the phyCAM-P connector if jumper J5 is set to 2+3.
- On the extension connector X2, pin 1

Pinout of the extension connector X2

Pin	Dir	Funktion
1	I	TRIGGER0_IN
2	-	GND (signal ground)
3	O	MONITOR_OUT

Table 24: VM-012 X2 – Extension Connector

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

4.7.7.3 Monitor out

The *MONITOR_OUT* signal can be configured to output either the *Monitor0* or the *Monitor1* signal of the VITA 1300 image sensor.:

Signal		Function	I/O	Configuration
MONITOR_OUT		**MONITOR0**	O	**J7:2-3**
		MONITOR1	O	J7:1-2

The *MONITOR_OUT* signal is available on the following connectors:

- *CAM_CTRL1* - pin 7 of the phyCAM-P connecor (optional, jumper setting: J11 = 2-3)
- pin 3 of the extension connector X2

The function of the monitor signal is set by the *MONITOR_SELECT* register of the image sensor.

Monitor configuration options (overview):

Function	Monitor0	Monitor1	Notes
0	x	x	constant low
Integration Time	x		1 during integration time
ROT Indication	x	x	‘1’ during ROT, ‘0’ outside
Dual/Triple Slope Integration		x	asserted during DS/TS FOT sequence
Start of x-Readout Indication	x	x	
Black Line Indication		x	‘1’ during black lines, ‘0’ outside
Frame Start Indication	x		
Start of ROT Indication		x	
First Line Indication	x		‘1’ during first line, ‘0’ for all others
Start of X-readout Indication for Black Lines	x		
Start of X-readout Indication for Image Lines		x	

(ROT = Row Overhead Time, FOT = Frame Overhead Time)

4.7.7.4 Reset

Applying a low-level (GND) at the reset input initiates a reset of the camera sensor. All registers are set to their default values.
The reset input should be connected to the /RESET output of the microcontroller board. Ensure that the /RESET signal is released after power up of the sensor. MCLK should be applied to the camera before /RESET is released.
The reset signal must be held on high-level during operation of the camera module.
Asserting the /RESET signal initiates a reset of the image sensor and switches the sensor supply voltages off. The sensor supply remains in off state until the /RESET signal is in active state (low).
When the /RESET signal is de-asserted (high state), access to the I²C registers of the VM-012 is possible after a delay of approx. 100 ms.

A sensor reset can also be initiated by software. For that the bit *AUTO_SENSOR_RESET* is set to 1. The bit is cleared automatically at the end of the sensor's reset cycle.

The image sensor can be held in reset state permanetly. During this state, the sensor's power supply is switched off. This can be used to reduce the power consumption of the camea module.
The sensor is brought in this state by setting the bit *SENSOR_RESET* to 1. The sensor remains in this state until the bit is cleared by software.
When the bit is cleared, the sensor's power supply is switched on again by the internal power controller and reset is deasserted. After approx. 100 ms the sensor can be accessed again.

Notes:
- After a sensor reset is performed, the contents of the sensor registers are set to default state.
- Neither read or write access of sensor registers may be performed while the image sensor is in reset state.

- The VM012 control- and status registers which are mapped into the sensor's registers (see 4.7.6.3) can be accessed even while the sensor is performing a reset or is held in reset state.

A complete reset of the camera module can be performed by:

- powering the camera module off and on again
- by software: Asserting bit *VM-012_RESET*

A complete reset of the camera module can be initiated by asserting bit *VM-012_RESET*. The image sensor and the internal microcontroller will perform a reset cycle.
All registers are set to their default state.
The bit *VM-012_RESET* is automatically cleared at the end of the reset cycle.

Note:
Changes to the I²C address of the camera module take effect only after a complete reset of the camera module has been performed.

4.7.7.5 Output-Enable

The output enable input (pin 32) is not implemented for the VM-012 camera module. Data- and control lines are always active.
The pin is connected internally to the microcontroller and has the same electrical characteristics as any other input pins.

4.7.7.6 I²C-EEPROM (optional)

As an option, a serial I²C EEPROM can be installed on the VM-012 camera module. For example the EEPROM can be used to store application data such as calibration data.
The EEPROM type is M24C02-RMC6TG. It features a size of 2 kBit.
The default I^2C-address of the EEPROM is 0xAE.
Other addresses can be selected by setting J13, J14 and J15 (see section 5.6.2).
Data transfer rate: 100 kHz Standard Mode / 400 kHz Fast Mode

For more information please refer to the EEPROM's datasheet.

4.7.7.7 Internal MCLK Oscillator

As an option, the camera board can be populated with a crystal oscillator. This allows the generation of the master clock MCLK on board so no external MCLK clock has to be fed into the board on pin 29 of the phyCAM-P connector.
For using the internal clock source, OZ1 must be populated and J1 must be set to 1+2 position.

4.7.8 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

5 Technical Specification phyCAM-S Camera modules

5.1 VM-006-BW-LVDS - phyCAM-S camera module
1.3 Mpixel / monochrome

5.1.1 Specifications

Features

- 1.3 Mpixel image sensor, monochrome
- phyCAM-S – serial interface
- Frame rate up to 30 fps
- Rolling shutter
- High dynamic range
- External trigger and strobe
- Secondary connector with trigger, strobe and I/O (optional)

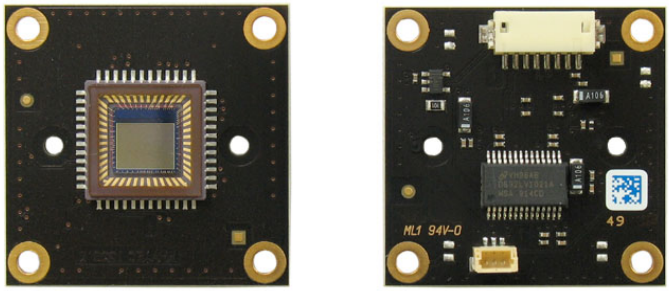


Figure68: phyCAM-S (VM-006-BW-LVDS) (front / rear view)

Parameters

	VM-006-BW-LVDS
Sensor	
Resolution	1.3 Mpixels
Pixels (H x V)	1280 x 1024
Sensor Size	1/2" 6.66 x 5.32 mm
Pixel Size	5.2 x 5.2 µm
Color / Monochrome	monochrome
Technology	CMOS
Image Sensor	Aptina MT9M001
Scan System	progressive
Shutter Type	rolling
Frame rate (fps) full resolution	up to 30 fps
Video Resolution	n/a
Responsivity	1.2 V/lux-sec
max. Dynamic Range	68.2 dB
High Dynamic Range	
Exposure Time	programmable
Gain	x1...x15
AEC	-
AGC	-
Gamma Correction	-
White Balance/AWB	n/a
Ext. Trigger / Sync.	Trigger / Strobe
ROI	yes
Skipping	2 / 4 / 8
Mirror	programmable
Image Processor	-
LED Lightning	-
Special Functions	see section 5.1.3

Electrical Interface	
Video Output Type	digital
Interface	phyCAM-S
Data Format	8-Bit serial
Interface-Mode	Y8
Dataline-Shifting	-
Camera Config. Bus	I²C
Supply Voltage	3.3 V
Power Consumption	538 mW
Pwr. Consumpt. Standby	100 mW*

Mechanical Parameters	
Lens Connector	none / M12 / C-CS
Lens	-
Housing	-
Dimensions (mm)	34 x 34
Mounting	4 x M2.5
Color (housing)	-
Weight (PCB)	7 g
Operating Temperature	0...70°C

Connectors	
Data and Power	Hirose 8-pin crimp
Trigger / Sync.	JST 3-pin crimp
Iris	-
Special functions	-

n/a: not applicable. All parameters are subject to change
*) depending on MCLK frequency

Table 25: phyCAM-S Parameters (VM-006-BW-LVDS)

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operating Current	I_{CAM}	-	156		mA
Input high voltage	V_{IH}	V_{CAM} -0.3	-	V_{CAM} +0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Output high voltage	V_{OH}	V_{CAM} -0.3	-	-	V
Output low voltage	V_{OL}	-	-	0.2	V
Voltage Set Resistor	R_{31}	-	0	2	Ω
Operating Temperature	T_{OP}	0	-	60	°C
Storage Temperature	T_{STG}	-30	-	85	°C

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	16	-	40	MHz
Clock Duty Cycle	$dutycyle_{MCLK}$	45	50	55	%
MCLCK to PCLK delay	t_{CP}	-	10	-	ns
PCLK to data valid	t_{PD}	-	-	1	ns
PCLK to Sync high	t_{PVH}	-	-	7	ns
PCLK to Sync low	t_{PVL}	-	-	13	ns
I²C Frequency	f_{I2C}	-	100	-	kHz

	Symbol	Min.	Typ.	Max.	Unit
LVDS-Serializer					
Output differential voltage	$\|V_{OD}\|$	200	270	-	mV
V_{OD} change between complementary out states	$\|DV_{OD}\|$	-	-	35	mV
Output offset voltage	V_{OS}	0.78	1.1	1.3	mV
V_{OS} change between complementary out states	DV_{OS}	-	-	35	mV
Output current when short to GND	I_{OS}	-	±30	±40	mA
Output current in Tri-State	I_{OZ}	-	±1	±10	µA
LVDS-Receiver					
Input differential, positive	V_{IDTH+}	-	-	100	mV
Input differential, negative	V_{IDTH-}	-	-100	-	mV
Shunt	R_{SHUNT}	-	100	-	Ω

Data Formats

Monochrome:

- Y8 : 8-bit grey scale

Spectral Characteristics

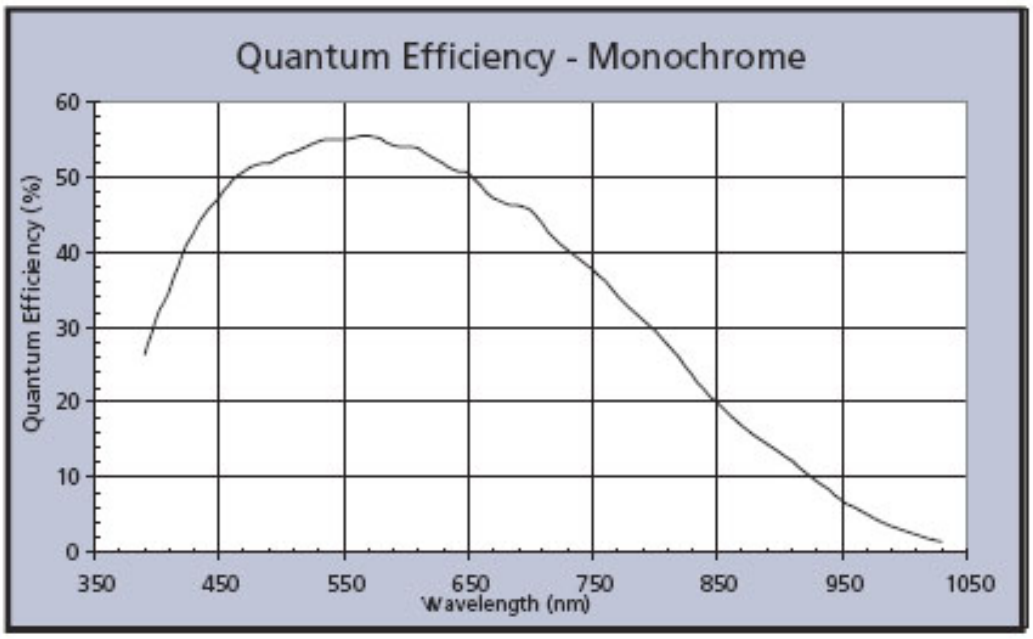


Figure69: phyCAM-S Spectral Characteristics (VM-006-BW-LVDS)

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

5.1.2 I²C Addresses

Device	I²C-Address	Configuration	Variant
Camera Sensor	0xBA		all

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with 7-bit Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

5.1.3 Special Features VM-006-BW-LVDS

5.1.3.1 Trigger

Using the trigger input allows precise control of the point in time an image is captured by an electrical signal. When the camera is in *snapshot-mode*, a high-level at the trigger input starts a capture process.

When using the *Continuous-Video Mode* (live image mode, default), the trigger input should be hold at low-level (GND) or left open. For details about the trigger mode, please refer to the sensor datasheet.

The trigger input is available at pin 3 of the extension connector.

5.1.3.2 Strobe

A high pulse at the strobe output indicates that the image array of the sensor has been reset. It indicates that the capture of an image has been completed. For details about the strobe signal, please refer to the sensor datasheet. The strobe signal is available on pin 4 of the expansion connector.

5.1.3.3 Expansion Connector

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	LED_OUT / STROBE

Table 26: phyCAM-S X104 Connector (VM-006-LVDS)

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

5.1.4 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website

for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

5.2 VM-007-LVDS - phyCAM-S camera module

Wide-VGA / monochrome, color

Note:
This part is not available for new designs.
Information given in this section is for reference use only.

5.2.1 Specifications

Features

- Wide-VGA sensor (360, 960 pixels)
- Monochrome (VM-007-BW-LVDS) *or* color (VM-007-COL-LVDS)
- phyCAM-S – interface
- Frame rate up to 60 fps
- Global shutter
- External trigger and strobe
- LED light (optional)
- Secondary connector with trigger, strobe and I/O (optional)

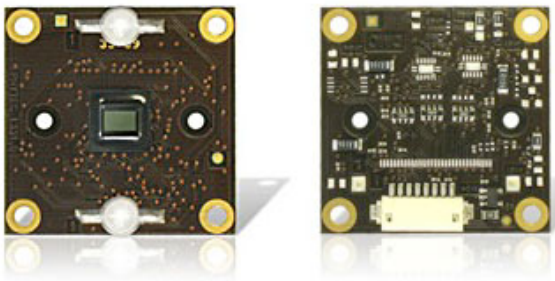


Figure70: phyCAM-S (VM-007-LVDS) (with LED-light, front- / rear view)

Parameters

	VM-007-BW-LVDS	VM-007-COL-LVDS
Sensor		
Resolution	WVGA	WVGA
Pixels (H x V)	752 x 480	752 x 480
Sensor Size	1/3" 4.51 x 2.88 mm	1/3" 4.51 x 2.88 mm
Pixel Size	6.0 x 6.0 µm	6.0 x 6.0 µm
Color / Monochrome	monochrome	color
Technology	CMOS	CMOS
Image Sensor	Aptina MT9V022	Aptina MT9V022
Scan System	progressive	progressive
Shutter Type	global	global
Frame rate (fps) full resolution	up to 60 fps	up to 60 fps
Video Resolution	n/a	n/a
Responsivity	4.8 V/lux-sec	4.8 V/lux-sec
Max. Dynamic Range	>55 dB linear	>55 dB linear
High Dynamic Range	>80...100 dB	>80...100 dB
Exposure Time	programmable	programmable
Gain	x1...x4	x1...x4
AEC	auto or manual	auto or manual
AGC	auto or manual	auto or manual
Gamma Correction	-	-
White Balance/AWB	n/a	manual
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	yes	yes
Binning	2x2 / 4x4	n/a
Mirror	programmable	programmable
Image Processor	-	-
LED Lightning	optional	optional
Special Functions	see section 5.2.3	see section 5.2.3

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-S	phyCAM-S
Data Format	8-Bit serial	8-Bit serial
Interface-Mode	Y8	8-Bit RGGB (Bayer)
Dataline-Shifting	-	-
Camera Config. Bus	I²C	I²C
Supply Voltage	3.3 V	3.3 V
Power Consumption	320 mW	320 mW
Pwr. Consumpt. Standby	100 µW	100 µW

Mechanical Parameters		
Lens Connector	none / M12 / C-CS	none / M12 / C-CS
Lens	-	-
Housing	-	-
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	-	-
Weight (PCB)	7 g	7 g
Operating Temperature	-25...85°C	-25...85°C

Connectors		
Data and Power	Hirose 8-pin. Crimp	Hirose 8-pin. Crimp
Trigger / Sync.	JST 3-pin Crimp	JST 3-pin Crimp
Iris	-	-
Special functions	-	-

n/a: not applicable. All parameters are subject to change.

Table 27: phyCAM-S Parameters (VM-007-LVDS)

Electrical Specifications (without LED light)

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operating Current	I_{CAM}	-	100	-	mA
Input high voltage	V_{IH}	V_{CAM} -0.5	-	V_{CAM} +0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Output high voltage	V_{OH}	V_{CAM} -0.7	-	-	V
Output low voltage	V_{OL}	-	-	0.3	V
Voltage Set Resistor	T_{OP}	-25	-	85	°C
Operating Temperature	T_{STG}	-25	-	85	°C

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	13	-	27	MHz
Clock Duty Cycle	$dutycyle_{MCLK}$	45	50	55	%
Data Setup-Time	t_{SD}	14	16	-	ns
Data Hold Time	t_{HD}	14	16	-	ns
I²C Frequency	f_{I2C}	-	100	-	kHz

	Symbol	Min.	Typ.	Max.	Unit
LVDS-Serializer					
Output differential voltage	$\|V_{OD}\|$	250	-	400	mV
V_{OD} change between complementary out states	$\|DV_{OD}\|$	-	-	50	mV
Output offset voltage	V_{OS}	1.0	1.2	1.4	mV
V_{OS} change between complementary out states	DV_{OS}	-	-	35	mV
Output current when short to GND	I_{OS}	-	±10	±12	mA
Output current in Tri-State	I_{OZ}	-	±1	±10	µA
LVDS-Receiver					
Input differential, positive	V_{IDTH+}	-	-	100	mV
Input differential, negative	$V_{IDTH–}$	-	-100	-	mV
Shunt	R_{SHUNT}	-	100	-	Ω

Data formats

Monochrome (VM-007-BW):

- Y8 : 8-bit grey scale

Color (VM-007-COL):

- RGGB (Bayer-Pattern) up to 8-bit color depth

Spectral Characteristics

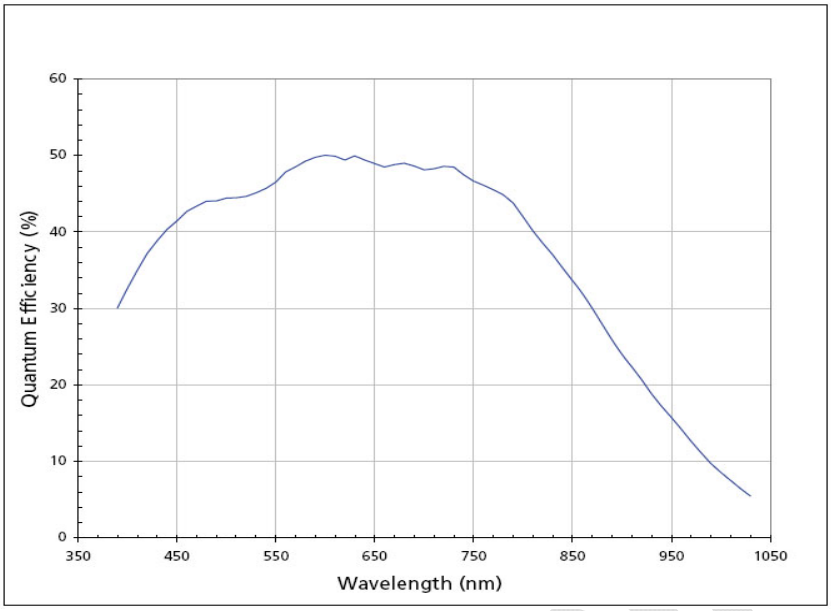


Figure71: phyCAM-S Spectral Characteristics (VM-007-BW-LVDS)

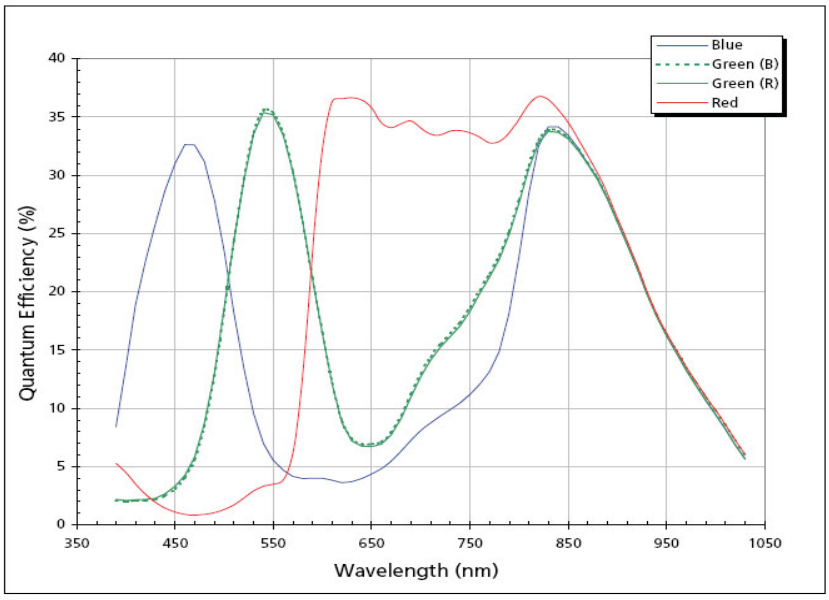


Figure72: phyCAM-S Spectral Characteristics (VM-007-COL-LVDS)

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

5.2.2 I²C Addresses

Device	I²C-Address	Configuration		Variant
		J102	J101	
Camera Sensor	0x90	**1-2**	**1-2**	all
	0x98	2-3	1-2	
	0xB0	1-2	2-3	
	0xB8	2-3	2-3	
LED - control	0x82			-LED

Default configuration (printed bold): 0x90

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

For the location of the jumpers see *Figure29*.

5.2.3 Special Features VM-007-LVDS

5.2.3.1 Windowing / Binning

To reduce the image resolution two functions of the camera can be used: Windowing and Binning. Which method is to be preferred depends on the application.:

- *Windowing:*
  Also called *Region of Interest* (ROI).
  Only a part of the sensor's pixel array is used for image aquisition. Pixels outside of this field are skipped. This method reduces the effecive size of the image sensor. This has to taken into consideration for calculation of the lens parameters focal length / angel of view.
  The origin of the ROI can be moved on the physical area of the image sensor. This allows electronical pan and tilt effects.
- *Binning:*
  Binning combines neighborhood pixels to one big pixel. This means the effective size of a pixel is increased while the number of pixel on the sensor is decreased. Binning improves the sensitivity of the sensor because the of the enlargement of the

pixel size.
On most color sensors that use the Bayer Pattern model, neighboring pixels cannot be combined because they have different color filters. See the sensor datasheet if the sensor supports binning on a color matrix.

5.2.3.2 Trigger

Using the trigger input allows precise control of the point in time an image is captured by an electrical signal. The trigger signal is generated externally, not on the camera module, and is fed to the camera by the EXPOSURE input.

The EXPOSURE signals can be used in several modes. See the Aptina MT9M022 or MT9V024 sensors datasheets for details. More information about snapshot mode can be found in the Aptina *TN0960_Snapshot* tech note.

Note: The EXPOSURE signal (*CAM_TRIG*) is available from PCB revision PL1331.0.

Please refer to section 4.2.5.3.1 for more information about the trigger function.

The trigger input is available at pin 1 of the extension connector X107. The CAM_TRIG signal is tied to low by a 4.7 kΩ resistor on the camera module. To release a trigger pulse, the signal must be driven to high state, V_{CAM} (3.3V).

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	LED_OUT / STROBE

Table 28: phyCAM-S X107 Connector (VM-007-LVDS)

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

5.2.3.3 Strobe / LED-OUT

The *Strobe / LED-OUT* output indicates the period of time when the sensor undergoes exposure. During active exposure, this output is active high. Please refer to *section 4.2.5.4* for more information.

5.2.3.3.1 Control of external light sources

The LED_OUT signal is also available at connector X107 (see *Table 28*). This allows connection of gated light sources directly to the camera module.

5.2.3.3.2 Controlling the internal LEDs by STROBE

The phyCAM-S VM-007-xxx-LVDS-LED variants feature two red 5mm LEDs (approx. 10.000 mcd, 630 nm). These LEDs can be controlled directly by the *Strobe/LED-OUT* signal.

This function can be deactivated either by:

- Hardware: open jumper J105
- Software: disable *LED_OUT Bit 0*, Reg 0x1B of the camera sensor

5.2.3.4 LED Lights

The phyCAM-S VM-007-xxx-LVDS-LED variants feature two red 5-mm LEDs with a brightness of approx. 10.000 mcd and a wavelength of 630 nm. These LEDs can be used to illuminate objects close to the camera, such as barcode labels.

Note:
The LED light is available with the PCB version and the M12 lens holder. Please refer to *section 4.2.5.7* for more information.

5.2.4 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website

for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

5.3 VM-008 - phyCAM-Analog Video Digitizer (LVDS)

Wide-VGA / monochrome, color

The VM-008 Video Digitizer module is suitable for both phyCAM-P and phyCAM-S interfaces.

Please refer to section 4.3 for a detailed description of this product.

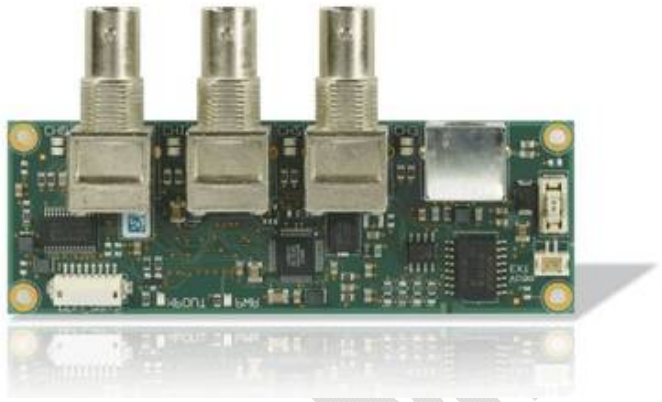


Figure73: Analog Video Digitizer VM-008

5.4 VM-009 – LVDS – phyCAM-S camera module
1.3 Mpixels / color / SOC

5.4.1 Specifications

Features

- 1.3 megapixel image sensor, color
- phyCAM-S – interface
- Frame rate up to 30 fps
- Rolling Shutter
- SOC – System on Chip: Integrated preprocessor
- RGB, YUV and RAW (Bayer pattern) output formats
- Integrated color- and gamma correction, sharpness enhancement, lens shade correction, digital zoom
- Automatic white balance (AWB) and auto black reference (ABR), auto flicker avoidance
- Fast exposure adaption
- Strobe output (fully automatic lightning control)
- Secondary connector for strobe output on the module (optional)

Figure74: phyCAM-S (VM-009-LVDS) (rear / front view)

Parameters

	VM-009-LVDS
Sensor	
Resolution	1.3 Mpixels
Pixels (H x V)	1280 x 1024
Sensor Size	1/3" 4.6 x 3.7 mm
Pixel Size	3.6 x 3.6 µm
Color / Monochrome	color
Technology	CMOS
Image Sensor	Aptina MT9M131
Scan System	progressive
Shutter Type	rolling
Frame rate (fps) full resolution	up to 30 fps
Video Resolution	n/a
Responsivity	1.0 V/lux-sec
Max. Dynamic Range	71 dB
High Dynamic Range	-
Exposure Time	programmable
Gain	programmable
AEC	yes
AGC	yes
Gamma Correction	yes
White Balance/AWB	yes / yes
Ext. Trigger / Sync.	Strobe
ROI	yes
Skipping	2 / 4
Mirror	programmable
Image Processor	yes
LED Lightning	-
Special Functions	sharpening, lens shade corr., color control...

Electrical Interface	
Video Output Type	digital
Interface	phyCAM-S
Data Format	LVDS
Interface-Mode	YUV, RGB-565, RGB-555, RGB-444, Raw RGGB (Bayer, processed)
Dataline-Shifting	-
Camera Config. Bus	I²C
Supply Voltage	3.3 V
Power Consumption	170 mW
Pwr. Consumpt. Standby	TBD.

Mechanical Parameters	
Lens Connector	none / M12 / C-CS
Lens	34 x 34
Housing	4 x M2.5
Dimensions (mm)	7 g
Mounting	-25...70°C

Connectors	
Data and Power	Hirose 8-pin crimp
Trigger / Sync.	JST 3-pin crimp

n/a: not applicable. All parameters are subject to change

Table 29: phyCAM-S Parameters (VM-009-LVDS)

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operating Current	I_{CAM}	-	-	160	mA
Input high voltage	V_{IH}	2.0	2.8	3.1	V
Input high voltage I²C	V_{IH_I2C}	2.0	3.3	V_{CAM} +0.3	V
Input low voltage	V_{IL}	-0.3	-	0.9	V
Output high voltage	V_{OH}	2,5	-	2,8	V
Output low voltage	V_{OL}	0	-	0.3	V
Operating Temperature	T_{OP}	-25	-	70	°C
Storage Temperature	T_{STG}	-30	-	80	°C

	Symbol	Min.	Typ.	Max.	Unit
Masterclock frequency	f_{MCLK}	-	-	54	MHz
Clock duty cycle	$dutycyle_{MCLK}$	40	50	60	%
MCLCK to PCLK delay	t_{CP}	7	9	15	ns
PCLK to data valid	t_{PD}	4	8	P	ns
PCLK to Sync high	t_{PVH}	4	8	P	ns
PCLK to Sync low	t_{PVL}	4	8	P	ns
Data Setup-Time	t_{SD}	4	8	P	ns
Data Hold Time	t_{HD}	4	8	P	ns
I²C Frequency	f_{I2C}	-	100	-	kHz

Note: P= ½ PCLK Period

	Symbol	Min.	Typ.	Max.	Unit
LVDS-Serializer					
Output differential voltage	$IV_{OD}I$	250	-	400	mV
V_{OD} change between complementary out states	$IDV_{OD}I$	-	-	50	mV
Output offset voltage	V_{OS}	1.0	1.2	1.4	mV
V_{OS} change between complementary out states	DV_{OS}	-	-	35	mV
Output current when short to GND	I_{OS}	-	±10	±12	mA
Output current in Tri-State	I_{OZ}	-	±1	±10	µA
LVDS-Receiver					
Input differential, positive	V_{IDTH+}	-	-	100	mV
Input differential, negative	V_{IDTH-}	-	-100	-	mV
Shunt	R_{SHUNT}	-	100	-	Ω

Data Formats

Monochrome:

- Y8 (processed)

Color:

- YCrCb 4:2:2
- RGB 565 (16-bit)
- RGB 555 (15-bit)
- RGB 444 (12-bit)
- ITU-R BT.656 marker-embedded
- RGGB (by color processor processed Bayer format)
- RGGB (Bayer format, raw sensor data)

Note:
Please note that the sensor must be configured so that the pixel clock *PCLK* is output continuously (no dropouts may occur). This is not the case in all modes of the sensor. Additional information can be found in the Aptina TN-09-163 Technical Note.

Please note the following limitations of the sensor modes on the phyCAM-S VM-009-LVDS:

- The internal scaler of the camera sensor cannot be used because it causes dropouts of the pixel clock. Instead, use the microprocessor's internal scaler or a software scaler.
- The internal scaler does not increase the frame rate, because the image is initially always completely exposed.
  To increase the frame rate, the skip-modes (skip2 = 4-fold faster skip4 = 8 times faster) must be used instead.
- The *Bayer Pattern 8-Bit* mode cannot be used because it causes dropouts of the pixel clock. Instead, use the *Bayer Pattern 8+2-Bit* mode and drop the lowest 2 bits.
- The *Bayer Pattern 10-Bit* mode cannot be used because the polarity of the pixel clock is inverted in this mode. Instead, use the *Bayer Pattern 8+2-Bit* mode.

- The low-power-mode of the sensor cannot be used. Instead, use the full-power-mode. The software drivers shipped with Development Kits are pre-configured for full-power-mode.

Spectral Characteristics

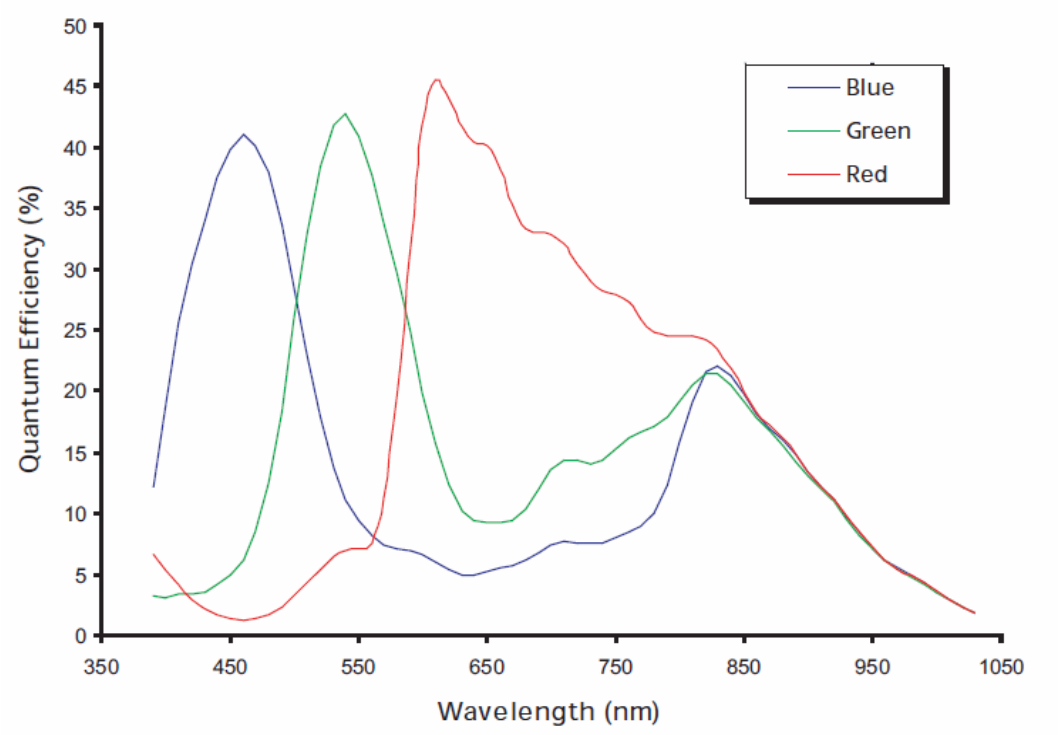


Figure75: Spectral Characteristics VM-009-LVDS

5.4.2 I²C Addresses

Device	I²C-Address	Configuration	Variant
		J101	
Camera Sensor	0x90	2-4	al
		1-2	
	0xBA	2-4	
		2-3	

Default setting (printed in bold):
0x90 (J101: 1-2)

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows

the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

For the location of the jumpers see *Figure46*.

5.4.3 Special Features VM-009-LVDS

5.4.3.1 Strobe

The strobe signal indicates the period of time the sensor array is in exposure mode. The output is pulsed high when the pixel array is sensitive to light. Please refer to section 4.4.5.1 for more information about this signal.

5.4.3.2 Image Processor

The integrated image flow processor (IFP) allows carrying out numerous pre-processing functions on the image on the camera module. Examples of these features include: gamma correction, color correction, sharpening, lens shading correction and on-the-fly defect correction.

Note:
Please refer to the datasheet of the camera sensor for detailed information.

5.4.4 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

5.5 VM-010-LVDS - phyCAM-S camera module

Wide-VGA / monochrome, color

5.5.1 Specification

Features

- Wide-VGA – sensor (360, 960 pixels)
- Monochrome (VM-010-BW-LVDS) *or* color (VM-010-COL-LVDS)
- phyCAM-S – interface
- Frame rate up to 60 fps
- Global shutter
- External Trigger and Strobe
- Secondary connector with trigger, strobe and I/O (optional)

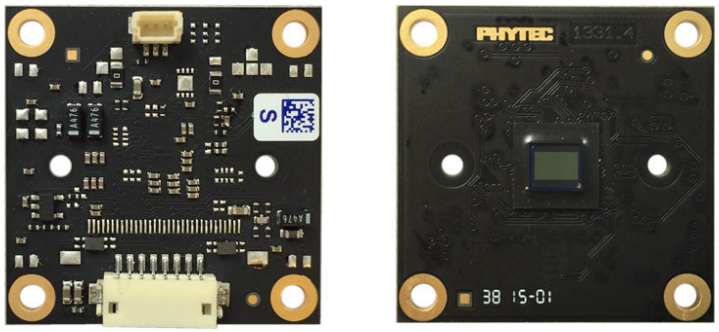


Figure76: phyCAM-S (VM-010-LVDS, PL-1331.4) (rear / front view)

Note:
The following description refers to versions PL1331.4 and higher. If you have an older version of this camera module please contact Phytec support to obtain the corresponding version of the manual L-748e_9.

Parameters

	VM-010-BW-LVDS	VM-010-COL-LVDS
Sensor		
Resolution	WVGA	WVGA
Pixels (H x V)	752 x 480	752 x 480
Sensor Size	1/3" 4.51 x 2.88 mm	1/3" 4.51 x 2.88 mm
Pixel Size	6.0 x 6.0 µm	6.0 x 6.0 µm
Color / Monochrome	monochrome	color
Technology	CMOS	CMOS
Image Sensor	Aptina MT9V024	Aptina MT9V024
Scan System	progressive	progressive
Shutter Type	global	global
Frame rate (fps) full resolution	up to 60 fps	up to 60 fps
Video Resolution	n/a	n/a
Responsivity	4.8 V/lux-sec	4.8 V/lux-sec
Max. Dynamic Range	>55 dB linear	>55 dB linear
High Dynamic Range	>100 dB	>100 dB
Exposure Time	programmable	programmable
Gain	x1...x4	x1...x4
AEC	auto or manual	auto or manual
AGC	auto or manual	auto or manual
Gamma Correction	-	-
White Balance/AWB	n/a	manual
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	yes	yes
Binning	2x2 / 4x4	n/a
Mirror	programmable	programmable
Image Processor	-	-
LED Lightning	-	-
Special Functions	see section 5.5.3	see section 5.5.3

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-S	phyCAM-S
Data Format	8-Bit serial	8-Bit serial
Interface-Mode	Y8	8-Bit RGGB (Bayer)
Dataline-Shifting	-	-
Camera Config. Bus	I²C	I²C
Supply Voltage	3.3 V	3.3 V
Power Consumption	300 mW	300 mW
Pwr. Consumpt. Standby	200 µW	200 µW

Mechanical Parameters		
Lens Connector	none / M12 / C-CS	none / M12 / C-CS
Lens	-	-
Housing	-	-
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	-	-
Weight (PCB)	7 g	7 g
Operating Temperature	-25...85°C	-25...85°C

Connectors		
Data and Power	Hirose 8-pin crimp	Hirose 8-pin crimp
Trigger / Sync.	JST 3-pin crimp	JST 3-pin crimp
Iris	-	-
Special functions	-	-

n/a: not applicable. All parameters are subject to change.

Table 30: phyCAM-S Parameters (VM-010-LVDS)

Electrical Specifications

	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operating Current	I_{CAM}	-	50	200	mA
Input high voltage	V_{IH}	V_{CAM} -1.4	-		V
Input low voltage	V_{IL}		-	1.3	V
Output high voltage	V_{OH}	V_{CAM} -0.3	-	-	V
Output low voltage	V_{OL}	-	-	0.3	V
Operating Temperature	T_{OP}	-25	-	85	°C
Storage Temperature	T_{STG}	-25	-	85	°C

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	13	26.6	27	MHz
Clock Duty Cycle	$dutycycle_{MCLK}$	45	50	55	%
Data Setup-Time	t_{SD}	14	16	-	ns
Data Hold Time	t_{HD}	14	16	-	ns
I²C Frequency	f_{I2C}	-	100	400	kHz

	Symbol	Min.	Typ.	Max.	Unit
LVDS-Serializer					
Output differential voltage	$\|V_{OD}\|$	250	-	400	mV
V_{OD} change between complementary out states	$\|DV_{OD}\|$	-	-	50	mV
Output offset voltage	V_{OS}	1.0	1.2	1.4	mV
V_{OS} change between complementary out states	DV_{OS}	-	-	35	mV
Output current when short to GND	I_{OS}	-	±10	-	mA
Output current in Tri-State	I_{OZ}	-	±1	-	µA
LVDS-Receiver					
Input differential, positive	V_{IDTH+}	-	-	100	mV
Input differential, negative	V_{IDTH-}	-	-100	-	mV
Shunt	R_{SHUNT}		100		Ω

Data Formats

Monochrome (VM-010-BW-LVDS):

- Y8 : 8-bit grey scale

Color (VM-010-COL-LVDS):

- RGGB (Bayer-Pattern) up to 8-bit color depth

Spectral Characteristics

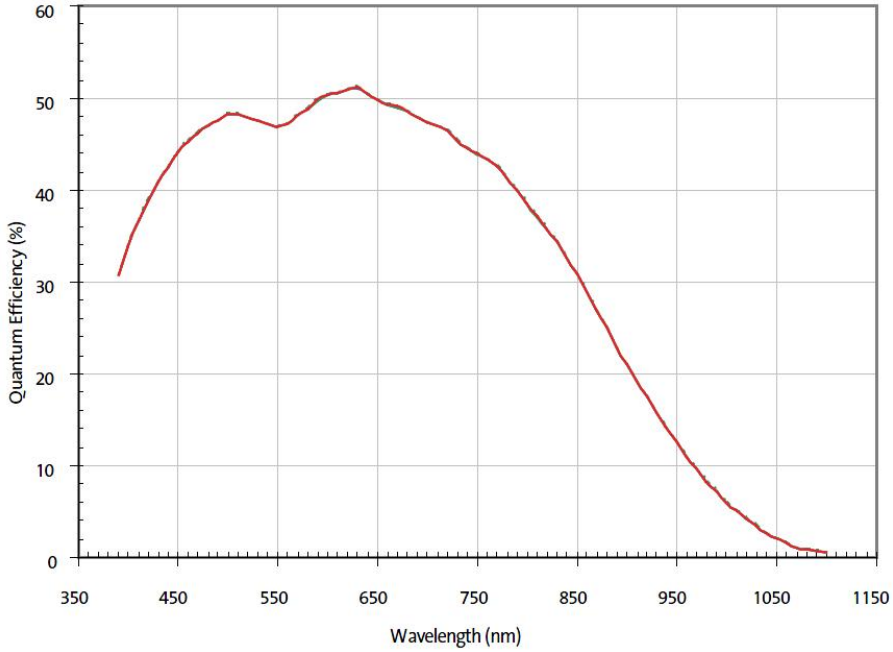


Figure77: Spectral Characteristics VM-010-BW-LVDS

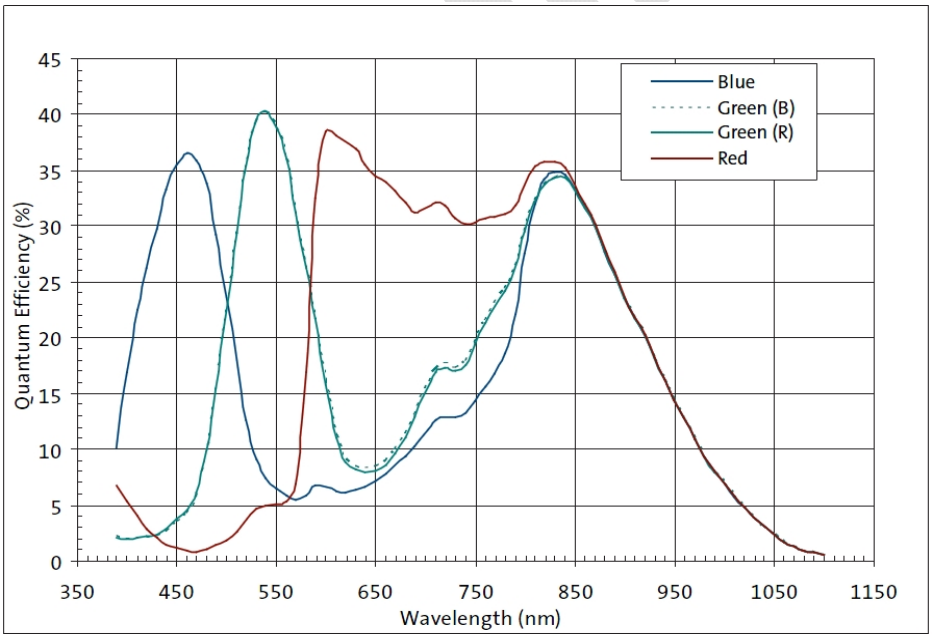


Figure78: Spectral Characteristics VM-010-COL-LVDS

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

5.5.2 I²C Addresses

Device	I²C-Address	Configuration		Variant
		J102	J101	
Camera Sensor	0x90	**1-2**	**1-2**	all
	0x98	2-3	1-2	
	0xB0	1-2	2-3	
	0xB8	2-3	2-3	
LED - Control	0x82			-LED

Default configuration (printed bold): 0x90

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

The locations of the jumpers are shown in *Figure51*.

5.5.3 Special Features

5.5.3.1 Windowing / Binning

To reduce the effective resolution of the sensor, windowing and binning can be used. The VM-010-LVDS module features the same methods as the VM-010. Please refer to section 4.5.5.1 for details.

5.5.3.2 Trigger

Using the trigger input allows precise control of the point in time an image is captured by an electrical signal.
The trigger function of VM-010-LVDS and VM-010 are indentical despite the fact that VM-010-LVDS features X107 connector only. Please refer to section 5.5.3.2 for more information about the trigger function.

5.5.3.3 Strobe / LED-OUT

The *Strobe / LED-OUT* output indicates the period of time when the sensor undergoes exposure. During active exposure, this output is active high.
The strobe function of VM-010-LVDS and VM-010 are indentical despite the fact that VM-010-LVDS features X107 connector only.
Please refer to section 4.5.5.3 for more information about this signal.

5.5.4 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

5.6 VM-011 – phyCAM-S+ camera module

5 MPixels, monochrome / color

5.6.1 Specification

Features

- 5 MPixels – sensor (5,038,848 pixels)
- monochrome (VM-011-BW-LVDS) or color (VM-011-COL-LVDS)
- phyCAM-S+ – interface
- Framerate 12.5 fps at full resolution
- Rolling Shutter
- External Trigger and Strobe
- Secondary connector with trigger and strobe (optional)

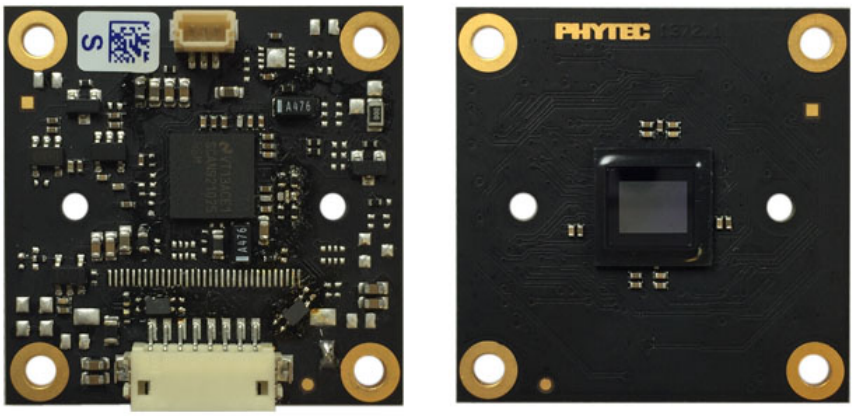


Figure79: VM-011-xxx-LVDS (phyCAM-S+, PL1372.1) (rear / front view)

Parameters

	VM-011-BW-LVDS	VM-011-COL-LVDS
Sensor		
Resolution	5 MPixels	5 MPixels
Pixels (H x V)	2592 x 1944	2592 x 1944
Sensor Size	1/2.5" 5.7 mm x 4.28 mm	1/2.5" 5.7 mm x 4.28 mm
Pixel Size	2.2 µm x 2.2 µm	2,2 µm x 2.2 µm
Color / Monochrome	monochrome	color
Technology	CMOS	CMOS
Image Sensor	Aptina MT9P031	Aptina MT9P006
Scan System	progressive	progressive
Shutter Type	rolling	Rolling
Fame rate (fps) full resolution	up to 12.5 fps	up to 12.5 fps
Responsivity	1.4 V/lux-sec	1.76 V/lux-sec
Max. Dynamic Range	70.1 dB	67.74 dB
High Dynamic Range	n/a	n/a
Exposure Time	programmable	programmable
Gain	programmable	programmable r
AEC	n/a	n/a
AGC	n/a	n/a
Gamma Correction	n/a	n/a
White Balance/AWB	n/a	manuell
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	yes	yes
Skipping	2x2 / 3x3	2x2 / 3x3
Binning	2x2 / 4x4	2x2 / 4x4
Mirror	programmable	programmable
Image Processor	n/a	n/a
LED-Light	n/a	n/a
Special feeatures	see section 4.6.5	see section 4.6.5

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-S+	phyCAM-P
Data Format	8 Bit serial LVDS	8 Bit serial LVDS
Interface-Mode	Y8	8 Bit RGGB (Bayer)
Dataline-Shifting	n/a	n/a
Camera Config. Bus	I²C	I²C
Supply Voltage	3,3 V	3.3 V
Power Consumption	700 mW	700 mW
Pwr. Consumpt. Standby	60 mW	60 mW

Mechanical Parameters		
Lens Connector	none / M12 / C-CS	none / M12 / C-CS
Lens	n/a	n/a
Housing	n/a	n/a
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	n/a	n/a
Weight (PCB)	5 g	5 g
Operating Temperature	-25...70°C	-25...70°C

Connectors		
Data and Power	Hirose 8 pin crimp	Hirose 8 pin crimp
Trigger / Sync.	JST 3 pin crimp	JST 3 pin crimp
Iris	n/a	n/a
Special functions	n/a	n/a

n/a: not applicable. All parameters are subject to change

Tabelle 31: Parameters VM-011-xxx-LVDS (phyCAM-S+)

Electrical Specifications

	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{CAM}	3.0	3.3	3.6	V
Operation Current	I_{CAM}	-	250	-	mA
Input high voltage[1]	V_{IH}	2.1	3.3	-	V
Input low voltage[1]	V_{IL}	-	0	0.7	V
Input high voltage[2]	$V_{IHTrigger}$	2	2.8	3.3	V
Input low voltage[2]	$V_{ILTrigger}$	-	0	0.8	V
Output high voltage[1]	V_{OH}	-	3.3	-	V
Output low voltage[1]	V_{OL}	-	0	0.3	V
Output high voltage[3]	$V_{OHStrobe}$	1.9	2.8	-	V
Output low voltage[3]	$V_{OLStrobe}$	-	0.16	0.4	V
Betriebstemperatur[4]	T_{OP}	-25	-	70	°C
Lagertemperatur[4]	T_{STG}	-25	-	70	°C

[1] CAM_SDA, CAM_SCL, I=±100µA
[2] CAM_TRIGGER
[3] CAM_STROBE
[4] -30°C without the optional Trigger/Strobe-connector X2

	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{MCLK}	20	-	80	MHz
Clock Duty Cycle	$dutycycle_{MCLK}$	40	50	60	%
Data Setup-Time	t_{SD}	0	19.9	59.9	ns
Data Hold Time	t_{HD}	0	0	0	ns
I²C Frequency	f_{I2C}	-	100	400	kHz

	Symbol	Min.	Typ.	Max.	Unit
LVDS-Serializer					
Output differential voltage	$\|V_{OD}\|$	200	290	-	mV
V_{OD} change between complementary out states	V_{OS}	1.05	1.1	1.3	mV
Output offset voltage	DV_{OS}	-	-	35	mV
V_{OS} change between complementary out states	I_{OS}	-	-56	-90	mA
Output current when short to GND	I_{OZ}	-10	±1	+10	µA
LVDS-Receiver					
Input differential, positive	V_{IDTH+}	-	-	100	mV
Input differential, negative	V_{IDTH-}	-100	-	-	mV
Shunt	R_{SHUNT}		100		Ω

Data Formats

Monochrome (VM-011-BW-LVDS):

- Y8 : 8-bit grey scale

Color (VM-011-COL-LVDS):

- RGGB (Bayer-Pattern) up to 8-bit color depth

Spectral Characteristics

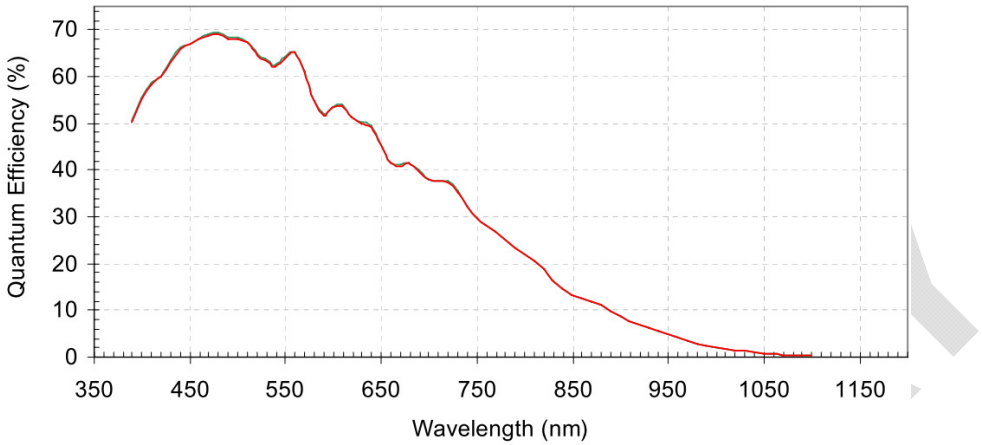


Figure80: Spectral Characteristics VM-011-BW-LVDS

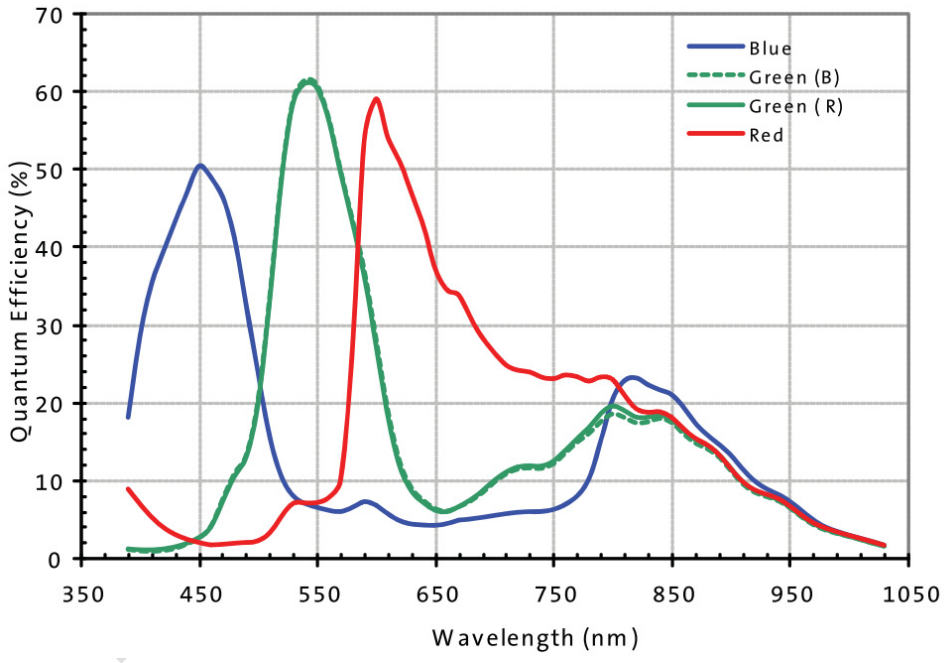


Figure81: Spektral Characteristics VM-011-COL-LVDS

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

5.6.2 I²C Addresses

Device	I²C-Address	Configuration	Variant
		J11	
Camera Sensor	**0x90**	**2+3**	all
	0xBA	1+2	

Device	I²C-Address	Configuration			Variant
		J13	J14	J15	
EEPROM	0xA0	1+2	1+2	1+2	all
	0xA2	2+3	1+2	1+2	
	0xA4	1+2	2+3	1+2	
	0xA6	2+3	2+3	1+2	
	0xA8	1+2	1+2	2+3	
	0xAA	2+3	1+2	2+3	
	0xAC	1+2	2+3	2+3	
	0xAE	**2+3**	**2+3**	**2+3**	

Default configuration of the camera sensor (printed bold): 0x90

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

5.6.3 Feature Pins

Signal	Pin	Funktion	I/O	Konfiguration
CAM_MCLK	29	**Master Clock**	**I**	**J16:2+4 (22Ω)**
		not active (internal)	-	J16:1+2 (22Ω)

Notes:
Configuration: Internal Configuration of the camera module to activate / use this feature.

If more than one feature is available for one pin, the default configuration is printed in **bold**.

NOMT = not mounted

In order to best meet technical requirements and cost objectives, custom configurations are available for high volume deliveries of phyCAM modules. Please consult PHYTEC for additional information.

By setting J16 to 1+2 position the master clock of the image sensor is fed from an optional internal osciallator (see section 5.6.5.5).
If the internal oscillator is used we recommend a customized variant of the camera module, where the clock receiver is not populated.

5.6.4 Jumper Map VM-011-xxx-LVDS

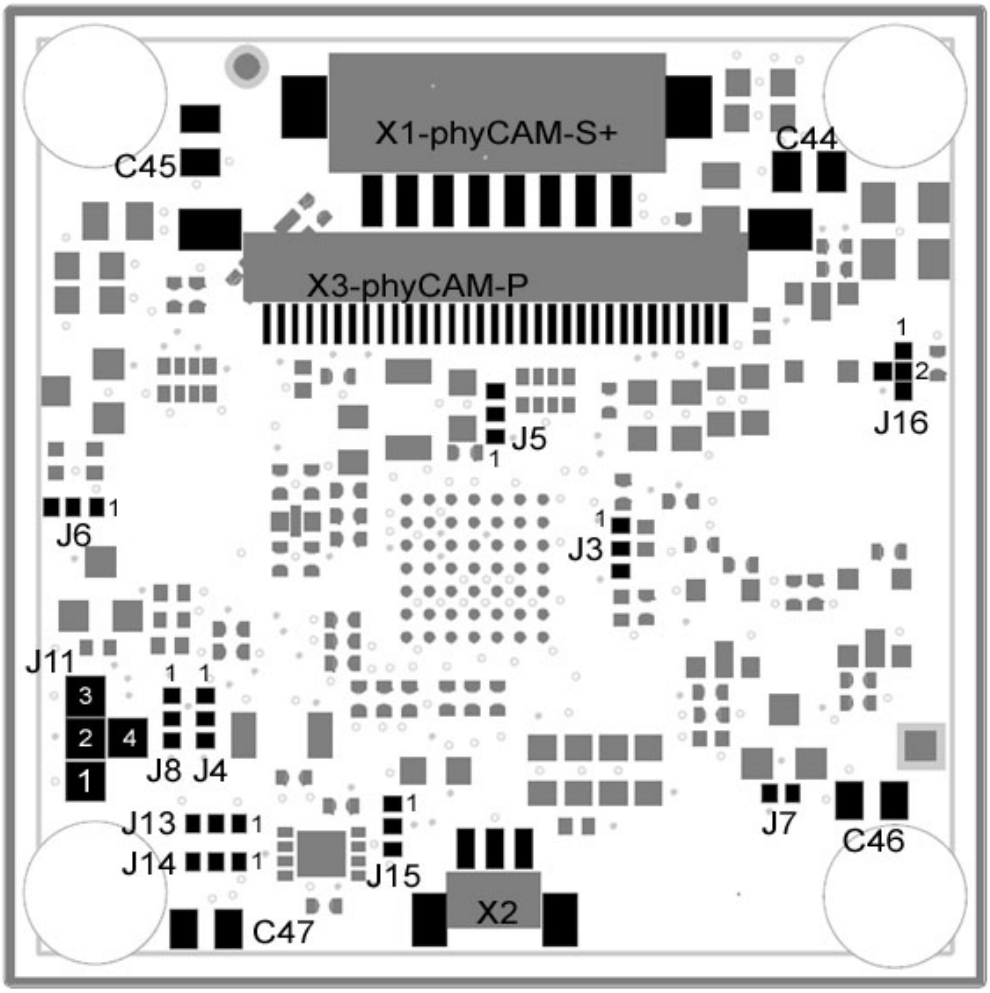


Figure82: Jumper Map VM-011-xxx-LVDS, PL1372.1

5.6.5 Special Features VM-011

5.6.5.1 Variable Resolution

As with other members of the phyCAM product family, the image resolution of the VM-011 module can be reduced virtually. This allows the user to adapt the captured image size and the amount of data sent to the microcontroller to the needs of the appliocation. Reducing the image resolution can also result in a higher framerate. The following table shows some examples for typical sub-resolutions for the VM-011 camera module:

	Resolution options			
Image Resolution	Name	max. Frame rate	Mode	Format
2592 x 1944	-	15	window	1/2.5"
2048 x 1536	QXGA	21	window	1/3"
1920 x 1080	FullHD	31	window	1/3"
1600 x 1200	UXGA	31	window	1/4"
1280 x 1024	SXGA	42	window	1/4.5"
1280 x 720	HD	60	binning	1/2.5"
1024 x 768	XGA	63	window	1/5.5"
		63	skipping	1/3"
		47	binning	1/3"
800 x 600	SVGA	90	window	1/6"
		90	skipping	1/4"
		65	binning	1/4"
640 x 480	VGA	123	window	1/6.5"
		123	skipping	1/2.5"
		53	binning	1/2.5"

Depending on the application's requriements different modes can be used to reduce the resolution:

- *window:*
  Only a part of the physical image sensor is used (*Region of Interest* – ROI). Pixels outside this window are skipped. This mode reduces the effective size of the image sensor. This must be taken into consideration when calculating the lens parameters for the system.

The start position of the ROI window can be moved on the physical image sensor field which allows electronical panning.

- *binning:*
  Binning combines adjacent pixels on the sensor. The effective pixel size is higher that the size of a single pixel. By this, the light sensitivity of the sensor is increased.
  For color sensors not the direct neighbor pixels are combined but the next pixels with the same color filter (see the datasheet of the sensor for details).
- *skipping:*
  During readout pixels in the image field are skipped. This reduces the image resolution but has hardly any impact on the effective sensor size. This can be helpful for lens selection or if switching between different modes is desired (electronical zoom).
  Compared to binning, skipping allows higher framerates.

5.6.5.2 Trigger / Bulb Exposure

This input allows precise control of the point in time an image is captured or the exposure time by an electrical signal:

- In Snapshot-Mode, this input controls the point in time an image is captured by the sensor. A low-level at the trigger input initiates an image capture.
- In Bulb Exposure-Mode the exposure time is controlled by this input..

More information about these modes can be found in the sensor datasheet.

The trigger input is available at the pin *CAM_CTRL2* of the phyCAM-P connector (J3 has to be set to 2-3 and J4 must be open).
This trigger input is also available at pin 1 of the extension connector X2.

Pin	Dir	Function
1	I	EXPOSURE / TRIGGER_IN
2	-	GND (Signal Ground)
3	O	STROBE

Table 32: VM-011 X2 Connector

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

Note
Polarity of the signal can be changed by programming the sensor's register.

5.6.5.3 Strobe

The *Strobe* output indicates the period of time when the sensor is undergoing exposure. When exposure is active, this output is active high.

More information about the strobe signal configuration can be found in the datasheet of the image sensor.

The signal is available at üin 3 of the extension connector X2.

5.6.5.4 I²C-EEPROM

As an option, a serial I²C EEPROM can be installed on the VM-011 camear module. The EEPROM can be used to store application data such as calibration data.
The EEPROM type is M24C02-RMC6TG. It features a size of 2 kBit.
The default I^2C-address of the EEPROM is 0xAE.
Other addresses can be selected by setting J13, J14 and J15 (see section 5.6.5.4).
Data transfer rate: 100 kHz Standard Mode / 400 kHz Fast Mode

For more information please refer to the EEPROM's datasheet.

5.6.5.5 Internal MCLK Oscillator

As an option, the camera board can be populated with a crystal oscillator. This allows the generation of the master clock MCLK on board so no external MCLK clock has to be fed into the board on pins 3 / 6 of the LVDS-connector X1.

For using the internal clock source, XT1 has to be populated and J16 must be populated with an 22 Ω resistor on 1+2 position.

5.6.6 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

5.7 VM-012 – phyCAM-S+ 1.3 MPixels Global Shutter – monochrome /color

5.7.1 Specification

Features

- 1.3 MPixels – sensor (1,310,720 pixels)
- monochrome (VM-012-LVDS-BW) or color (VM-012-LVDS-COL)
- phyCAM-S+ – interface
- Framerate: 37 fps at full resolution
- Framerate: 130 fps at VGA resolution
- Global Shutter and Rolling Shutter (selectable)
- Externer Trigger and Strobe
- Secondary connector with trigger and strobe (optional)

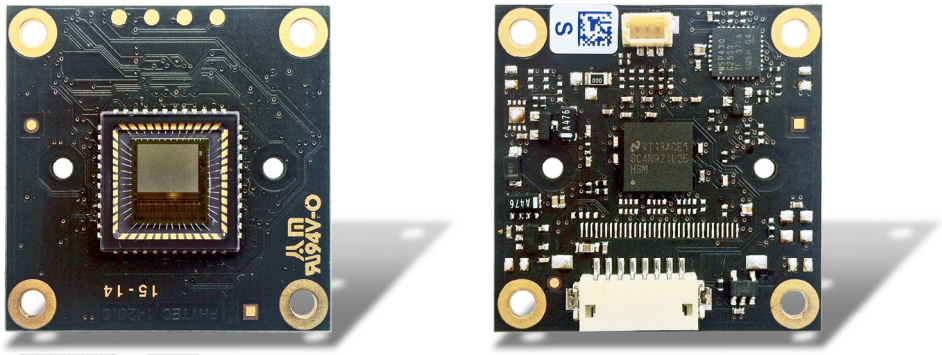


Figure83: VM-012 (phyCAM-S+) (front/ rear view)

Parameters

Funktion	VM-012-LVDS-BW	VM-012-LVDS-COL
Sensor		
Resolution	1.3 MPixels	1.3 MPixels
Pixels (H x V)	1280 x 1024	1280 x 1024
Sensor Size	1/2" 6.18 mm x 4.95 mm	1/2" 6.18 mm x 4.95 mm
Pixel Size	4.8 µm x 4,8 µm	4.8 µm x 4.8 µm
Color / Monochrome	monochrome	color
Technology	CMOS	CMOS
Image Sensor	ON Semiconductor VITA 1300 (NOIV2SN1300A-QDC)	ON Semiconductor VITA 1300 (NOIV2SE1300A-QDC)
Scan System	progressive	progressive
Shutter Type	global or rolling	global or rolling
Fame rate (fps)	37 fps (full resolution)	37 fps (full resolution)
	130 fps (VGA resolution)	130 fps (VGA resolution)
Responsivity	4,6 V/lux·sec (at 550 nm)	4,6 V/lux·sec (at 550 nm)
Max. Dynamic Range	60 dB (Rolling Shutter Mode) 53 dB (Global Shutter Mode)	60 dB (Rolling Shutter Mode) 53 dB (Global Shutter Mode)
High Dynamic Range	90 dB	90 dB
Exposure Time	programmable	programmable
Gain	programmable	programmable
AEC	automatic and manual	automatic and manual
AGC	automatic and manual	automatic and manual
Gamma Correction	n/a	n/a
White Balance/AWB	n/a	n/a
Ext. Trigger / Sync.	Trigger / Strobe	Trigger / Strobe
ROI	up to 8	up to 8
Skipping	2x2	2x2
Binning	2x2	2x2
Mirror	n/a	n/a
Image Processor	n/a	n/a
LED-Light	n/a	n/a
Special features	see section 4.7.7	see section 4.7.7

Electrical Interface		
Video Output Type	digital	digital
Interface	phyCAM-S+	phyCAM-S+
Data Format	8 Bit serial LVDS	8 Bit serial LVDS
Interface-Mode	Y8	8 Bit RGGB (Bayer)
Dataline-Shifting	n/a	n/a
Camera Config. Bus	I²C	I²C
Supply Voltage	3.3 V	3.3 V
Power Consumption	620 mW	620 mW
Standby Power	85 mW	85 mW

Mechanical Parameters		
Lens Connector	without / M12 / C-CS	without / M12 / C-CS
Lens	n/a	n/a
Housing	n/a	n/a
Dimensions (mm)	34 x 34	34 x 34
Mounting	4 x M2.5	4 x M2.5
Color (housing)	n/a	n/a
Weight (PCB)	5 g	5 g
Operating Temperature	-25...85°C	-25...85°C

Connectors		
Data and Power	Hirose 8 pol. Crimp	Hirose 8 pol. Crimp
Trigger / Sync.	JST 3 pol. Crimp	JST 3 pol. Crimp
Iris	n/a	n/a
Special functions	n/a	n/a

n/a: not applicable. All parameters are subject to change

Table 33: Parameters VM-012-xxx-LVDS (phyCAM-S+)

Electrical Specifications

	Symbol	min.	typ.	max.	Unit
Operating Voltage	V_{CAM}	3,0	3,3	3,6	V
Operating Current	I_{CAM}	-	200	-	mA
Input high voltage[1]	V_{IH}	2	-	V_{CAM} +0,3	V
Input low voltage[1]	V_{IL}	-0,3	-	0,8	V
Output high voltage[1]	V_{OH}	2,8	-	-	V
Output low voltage[1]	V_{OL}	-	-	0,2	V
Operating Temperature[2]	T_{OP}	-25	-	70	°C
Storage Temperature[2]	T_{STG}	-25	-	70	°C

[1] CAM_SDA, CAM_SCL, I=+/-100µA

[2] auf -30°C without the optional Trigger/Strobe-connector X2

	Symbol	min.	typ.	max.	Unit
Master Clock Frequency	f_{MCLK}	20	-	62	MHz
Clock Duty Cycle	$dutycycle_{MCLK}$	40	50	60	%
I²C Taktrate[2]	f_{I2C}	-	100	400	kHz

[2] the I²C master must support Clock-Stretching

	Symbol	min	typ	max	Unit
LVDS-Driver					
Output differential voltage	$IV_{OD}I$	200	290	-	mV
Output offset voltage	V_{OS}	1,05	1,1	1,3	mV
V_{OS} change between complementary out states	DV_{OS}	-	-	35	mV
Output current when short to GND	I_{OS}	-	-56	-90	mA
Output current in Tri-State	I_{OZ}	-10	±1	+10	µA
LVDS-Receiver					
Input differential, positive	V_{IDTH+}	-	-	100	mV
Input differential, negative	V_{IDTH-}	-100	-	-	mV
Termination resistor	R_{SHUNT}		100		Ω

Data Formats

monochrome (VM-012-BW-LVDS):

- Y8 : 8 bit grey scale

color (VM-012-COL-LVDS):

- RGGB (Bayer-Pattern) 8 bit color depth

Spectral Characteristics

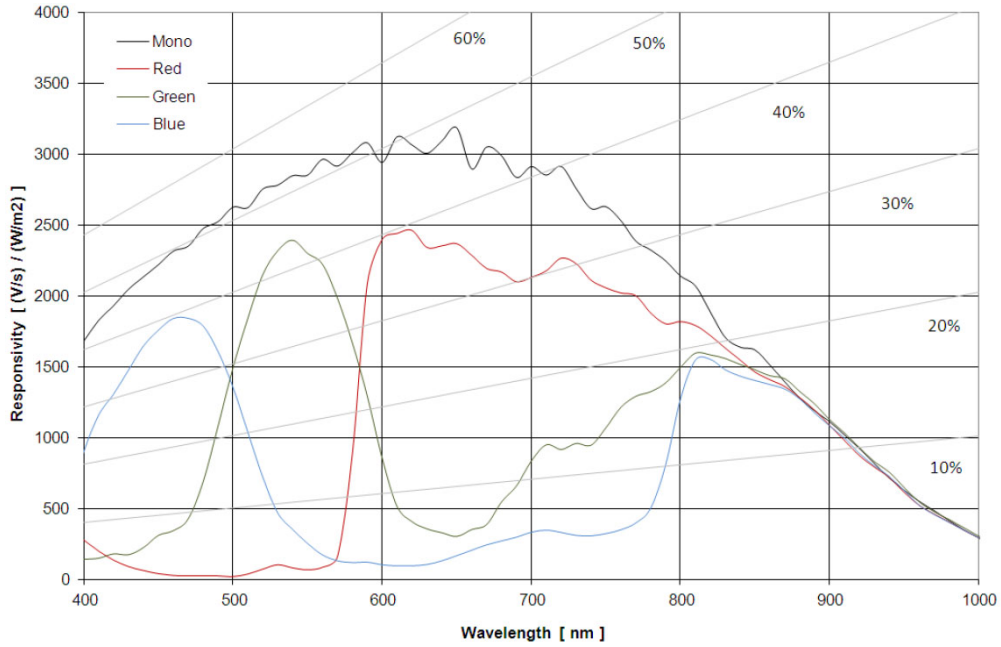


Figure84: Spektral Characteristics VM-012-BW / COL

Note:
Please refer to the datasheet of the camera sensor for detailed characteristics.

5.7.2 I²C Addresses

Device	I²C-Address	Configuration		Variant
		J9	J10	
Camera Sensor	**0x90**	**2+3**	**1+2**	all
	0x98	1+2	1+2	
	0xB0	2+3	2+3	
	0xB8	1+2	2+3	

Device	I²C-Address	Configuration			Variant
		J2	J3	J4	
EEPROM	0xA0	1+2	1+2	1+2	optional
	0xA2	2+3	1+2	1+2	
	0xA4	1+2	2+3	1+2	
	0xA6	2+3	2+3	1+2	
	0xA8	1+2	1+2	2+3	
	0xAA	2+3	1+2	2+3	
	0xAC	1+2	2+3	2+3	
	0xAE	**2+3**	**2+3**	**2+3**	

Default configuration of the camera sensor (printed bold):
0x90

I²C-addresses are shown in hexadecimal, 8-bit notation. Please note that Linux possibly uses 7-bit notation. If developing with Linux notation, shift the address value one bit to the right. The table shows the write address (bit 0 = 0). To read from the device, add one to the address (bit 1 = 1).

5.7.3 Jumper Map VM-012-xxx-LVDS

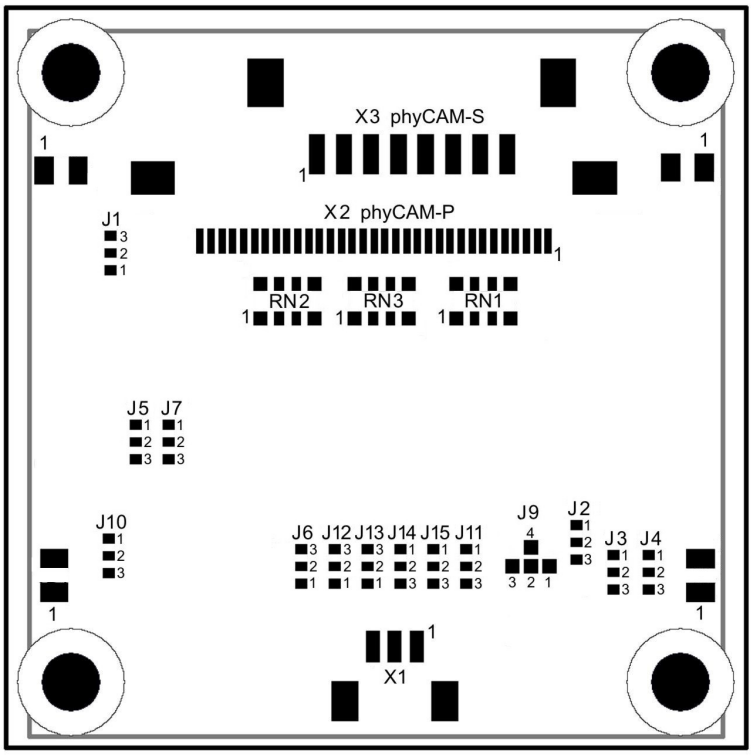


Figure85: Jumper Map VM-012-xxx-LVDS, PL1420.0

5.7.4 Pixel Remapping VM-012

The pixels of the VITA 1300 image sensor are organized in kernels. This means that the readout sequence of the pixels in a line is not sequentially consecutive as one would assume from the physical position of the pixel on the sensor.
The kernel size is 8 pixels in x-direction by 1 pixel in y-direction. Figure62 indicates how the kernels are organized.

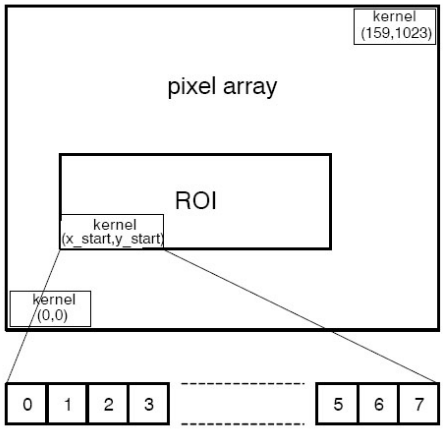


Figure86: Kernel organization in pixel array (VM-012)

The data order of the image data on the output channels depends on the subsampling mode:

(a) no subsampling

The pixel sequence is different for even and odd kernels like shown in Figure63:

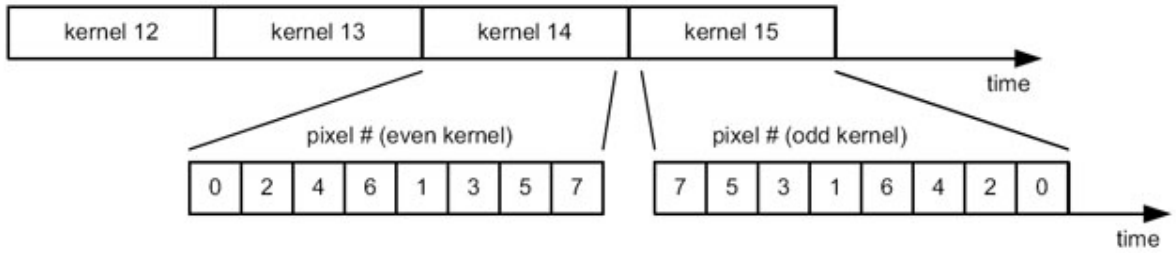


Figure87: Pixel order with no subsampling (VM-012)

(b) subsampling, monochrome sensor

In subsampling mode two adjacent kernels are combined to one single kernel (see figure below). By this the number of pixels are reduced by two. Only the pixels at the even pixel positions inside that kernel are read out. Figure64 shows the data order.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no-subsampling’ readout.

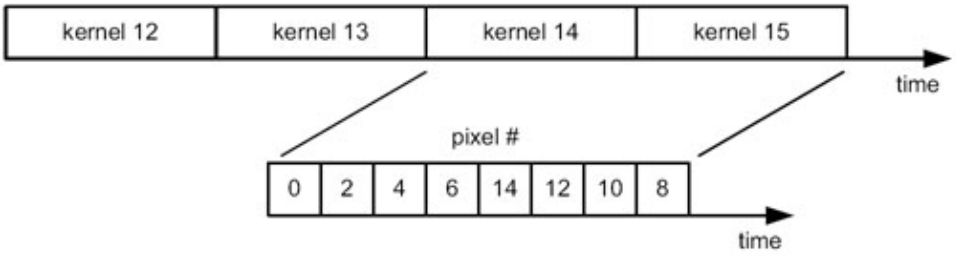


Figure88: Pixel order with subsampling, monochrome sensor

(c) subsampling, color sensor

In subsampling mode two adjacent kernels are combined to one single kernel (see figure below). By this the number of pixels are reduced by two. Only the pixels 0, 1, 4, 5, 8, 9, 12, and 13 are read out. Figure75 shows the data order.
Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no-subsampling’
readout.

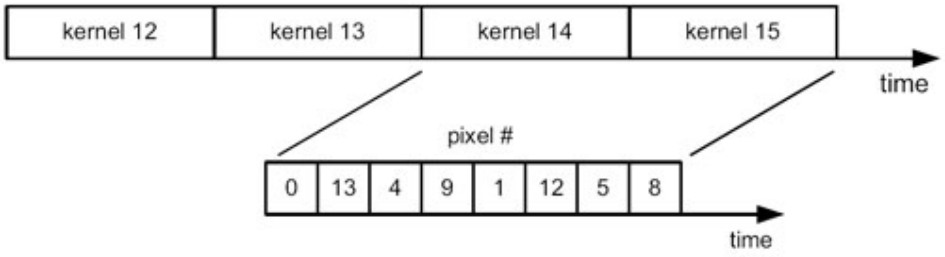


Figure89: Pixel order with subsampling, color sensor

Notes
The following processing unit must re-order the pixel seqence (for example by software) or the pixel order described above must be taken into consideration when processing the image data.

If ROIs are defined the borders of the ROI window must meet the borders of the kernels. Ideally the beginning of the ROI window is aligned in a way that it meets the same kernel type (even kernels).

Note
With the development kits Phytec ships a library and a GStreamer-function for pixel remapping.
See the Application Note „VM-012 Remapping“ for more details.

5.7.5 I²C Interface VM-012

For communication with the components on the camera module (like image sensor, EEPROM, etc.) the phyCAM interface features an I²C interface. I²C communication is used for phyCAM-P and phyCAM-S(+) also.
Via the I²C interface the CPU can read and write the registers of the camera sensor. By that the configuration of the sensor can be set.
In contrast to the phyCAM interface the VITA 1300 sensor uses a SPI interface for sensor control. On the VM-012 camera an additional microcontroller is used to translate the I²C bus of the phyCAM interface to SPI. This allows the VM-012 to be compatible to the phyCAM-P and phyCAM-S+ standard.
Because of the bus translation some particularites in I²C communication have to be considered.

The I²C interface of the VM-012 is organized in 8-bit data blocks:

- 8-Bit device address
- 8-Bit register address
- 2 x 8-Bit data

I²C access is always carried out by a 16-bit write or 16-bit read protocol.
According to the I²C specification the selection between read and write access is determined by the LSB of the device address.

- write access: LSB of the device address = 0
- read access: LSB of the device address = 1

5.7.5.1 16-Bit Write Sequence

Figure66 shows a typical sequence for writing a value into a 16 bit register. The master initiates the sequence by a start bit, followed by the register address and two data bytes. The byte order is most significant byte first.

After each byte an acknowledge (ACK) is sent by the VM-012. After the transmission of all 16 data bits the register content is updated. The master finishes the write cycle by sending a stop bit.

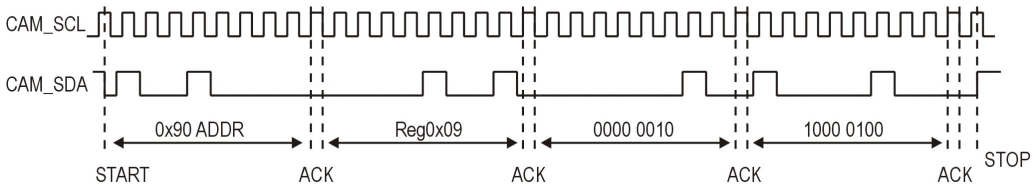


Figure 90: Writing the value 0x0284 into register 0x09 of device 0x90

Note
The data transmitted by the I²C write cycle are written into the register of the camera sensor after the write cycle is completed.
For that, an internal SPI bus cycle is executed.

Before a new I²C access is initiated the master has to wait until the internal SPI bus cycle ic completed.
To ensure this, one of the two methods described below can used:

Method 1:
After an I²C write access the master waits a given time before he starts the next I²C access to the camera. With firmware version V0.4 of the VM-012 the minimum waiting period time after the end of an I²C write access to the camera is 250µs.

Method 2:
The status flag *SPI_WRITE* in the register *VM012_STATUS* (0x99) can be used to determine the end of the internal write cycle.
This status flag is controlled by the internal microcontroller of the camera module..
The bit is set after a write command is detected. It is reset after the completion of the internal write cycle.
The status register is described in the next section.

Note
The registers VM012-STATUS, VM012-CONTROL and VM012_FIRMWARE can be accessed any time without any waiting

period. Especially this registers can be accessed while an interal write cycle is in progress.

5.7.5.2 16-Bit Read Sequence

A typical 16-bit read sequence is shown in Figure67. First the master has to write the register address, as in a write sequence. Then a start bit and the device address with LSB set specifies that a read is about to happen from the register. Note that the LSB set in the device address indicates read access.
With the following clocks the camera module outputs two data bytes which contain the 16 bit register content, high-byte first. After each 8 bit width Byte the master sends an acknowledge bit (ACK). The data transfer is finished by the master by sending a No-Acknowledge-Bit (NACK) after 16 bits of data have been transferred.

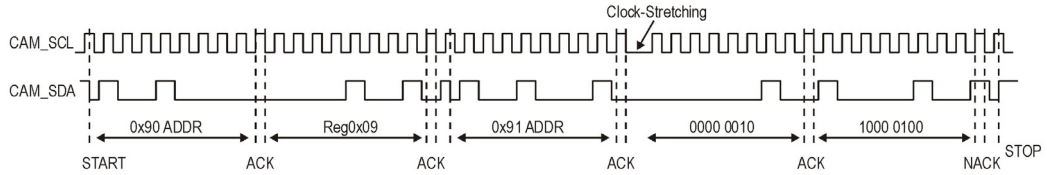


Figure 91: Reading the value 0x0284 from register 0x09 of device 0x90

Note:
No waiting time is needed after the initial write command of a read sequence. The following read command can be sent immediately.

After the internal microcontroller of the VM-012 has received the internal I²C write command and the device address with read bit set, it takes approx. 200µs to process the command internally. The master of the I²C has to wait this time before he can start reading the data from the camera module.
For this the VM-012 uses the „*Clock-Stretching*“ method. „*Clock-Stretching*“ is used only before the first data byte. The secons byte is transferred immediately.

Note:
The I²C-Master must support *Clock-Stretching*.

5.7.5.3 VM-012 Internal I²C Registers

5.7.5.3.1 Paging

The camera sensor VITA 1300 of the VM-012 has a register map with in total 511 registers. However many I²C routines support a register space of 255 registers only.
To allow easy access to all sensor registers by all systems, the VM-012 uses paging. By that the I²C-adress space is split into two pages of 255 registers. A page bit is used to select beteween lower and higher address space:

page bit	I²C-address sent to VM-012	acessed register of the VITA 1300 camera sensor
0	0x00 ... 0xFF	0x000 ... 0x0FF
1	0x00 ... 0xFF	0x100 ... 0x1FF

The sensor register accessed can be calculated by the following equation:

```
sensor_register = page_bit · 0x100 + I²C_register_address
```

The *PAGE_BIT* is located in the *VM012_CONTROL* register.

Note:
A description of the sensor's registers can be found in the VITA 1300 datasheet.

5.7.5.3.2 Control- and Status Registers

Note:
The following information refer to firmware version V0.5

Three additional registers are inserted into the register map of the camera sensor to control the internal microcontroller of the VM-012 and to read status informations.

Read and write accesses to this registers are processed by the microcontroller of the VM-012. These acesses are not passed to the VITA 1300 image sensor.
Because this three addresses are not uses by the VITA 1300, this does not interfere with any functions of the sensor.

VM-012 I²C Register Address	Page-Bit	Read	Description
0x97	x	R	Firmware-Version der VM-012
0x98	x	R/W	VM_012_CONTROL Register
0x99	x	R	VM_012_STATUS Register

x = don't care, R = read only, R/W = read and write access

Note:
This three registers are processed directly by the microcontroller of the VM-012. They are not transmitted via SPI to the image sensor. Therefore, no delay or waiting time is needed when accessing this registers..

Register description VM012_FIRMWARE; 0x97 (151 decimal)

0x97 – VM012_FIRMWARE					
Bit	**Bit Name**	**Bit Description**	**Default Hex (Dec)**	**Legal Values (Dec)**	**Read/ Write**
7...0	MINOR_REVISION	Firmware revision (minor part)	-	0...255	R
15...8	MAJOR_REVISION	Firmware revision (major part)	-	0...255	R

Register description VM012_CONTROL; 0x98 (152 decimal)

0x98 – VM012_CONTROL					
Bit	**Bit Name**	**Bit Description**	**Default Hex (Dec)**	**Legal Values (Dec)**	**Read/ Write**
0	PAGE_BIT	Page selection of the image sensor register: 0 = access registers 0x000 ... 0x0FF 1 = access registers 0x100 ... 0x1FF The page bit does not change its state after a camera reset.	0	0 ; 1	R/W
1	AUTO_SENSOR_RESET	Auto Software image sensor reset 0 = default state 1 = excecute camera sensor reset cycle Writing a 1 to this bit initiates an automatic reset cycle of the image sensor. The reset signal of the sesor is asserted and the sensor's power supply is switched off. After a delay of 100ms the sensor is powered up again and sensor reset is deasserted. This bit is reset automatically after the sensor reset cycle has finished.	0	0 ; 1	R/W
2	SENSOR_RESET	Image sensor reset 0 = default state 1 = image sensor reset Writing a 1 to this bit asserts the reset signal of the image sensor and the sensor's power supply is switched off. The image sensor is kept in this state until the bit is reset to 0. Resetting this bit to 0 will power up the sensor and deassert the sensor reset. This function can be used as a power saving state.	0	0 ; 1	R/W
3...7	RESERVED	reserved	-	-	-
8	VM-012_RESET	Camera module reset 0 = default state 1 = excecute camera module reset cycle Writing a 1 to this initiates a camera module reset cycle. A reset of the camera sensor and of the internal microcontroller is performed. After the reset cycle all registers are set to their default values.	0	0 ; 1	R/W
9...15	RESERVED	reserved	-	-	-

Register description VM012_STATUS; 0x99 (153 decimal)

0x99 – VM012_STATUS					
Bit	**Bit Name**	**Bit Description**	**Default Hex (Dec)**	**Legal Values (Dec)**	**Read/ Write**
0	SPI_READ	0 = SPI-READ idle 1 = SPI-READ in progress – only registers 0x97, 0x98 and 0x99 may be accessed. Note: If clock stretching is used, I²C read delay is inserted automatically. In this case it's not necessary to observe this status bit.	0	0 ; 1	R
1	SPI_WRITE	0 = SPI-WRITE idle 1 = SPI-WRITE in progress. While this bit is set, only registers 0x97, 0x98 und 0x99 may be accessed.	0	0 ; 1	R
2..15	RESERVED	reserved	-	-	-

5.7.6 Special Features VM-012-xxx-LVDS

5.7.6.1 Windowing / ROI

As with other members of the phyCAM product family, the image resolution of the VM-012-xxx-LVDS module can be reduced virtually. This means that only the user-selected Regions Of Interest (ROI) are read out.
This allows the user to adapt the captured image size and the amount of data sent to the microcontroller to the needs of the appliocation. Reducing the image resolution can also result in a higher framerate.

Abhängig von der Betriebsart können mehrere ROIs definiert werden:

- In global shutter mode, up to eight ROIs can be configured.
- In rolling shutter mode, only a single ROI is supported.

Note that if multiple ROIs are active, the pixel output order is determined by the physical position of the corresponding pixel on the sensor. This means that ROIs are masking the sensor, but they do not change the output seqence of the pixel data. Depending on the position of the multiple ROIs, the active pixels of the ROIs are nested.

5.7.6.2 Trigger

The trigger input can be configured in two ways:

- Triggered Shutter Master Mode
  In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting.

- Pipelined Shutter Slave Mode
  In this mode, the start of the integration and the integration time is controlled by the trigger signal.
  Integration starts with a rising edge of the trigger signal and is ended with the falling edge.

Note:
Trigger may not be activated during the Frame Overhead Time (FOT). The signal *First Line Indication* can be used to detect the image start. *First Line Indication* is a configuration mode of the *Monitor* signal (see 5.7.6.3).
Details of the trigger function are described in the datasheet of the image sensor VITA 1300.

The trigger input is available the extension connector X2, pin 1

Pinout of the extension connector X2

Pin	Dir	Funktion
1	I	TRIGGER0_IN
2	-	GND (signal ground)
3	O	MONITOR_OUT

Table 34: VM-012 X2 – Extension Connector

Connector type: JST BM03B-SRSS-TB
Matching header: JST SHR-03V-S

5.7.6.3 Monitor out

The *MONITOR_OUT* signal can be configured to output either the *Monitor0* or the *Monitor1* signal of the VITA 1300 image sensor.:

Signal		Function	I/O	Configuration
MONITOR_OUT		**MONITOR0**	O	**J7:2-3**
		MONITOR1	O	J7:1-2

The *MONITOR_OUT* signal is available on pin 3 of the extension connector X2

The function of the monitor signal is set by the *MONITOR_SELECT* register of the image sensor.

Monitor configuration options (overview):

Function	Monitor0	Monitor1	Notes
0	x	x	constant low
Integration Time	x		1 during integration time
ROT Indication	x	x	‘1’ during ROT, ‘0’ outside
Dual/Triple Slope Integration		x	asserted during DS/TS FOT sequence
Start of x-Readout Indication	x	x	
Black Line Indication		x	‘1’ during black lines, ‘0’ outside
Frame Start Indication	x		
Start of ROT Indication		x	
First Line Indication	x		‘1’ during first line, ‘0’ for all others
Start of X-readout Indication for Black Lines	x		
Start of X-readout Indication for Image Lines		x	

(ROT = Row Overhead Time, FOT = Frame Overhead Time)

5.7.6.4 Reset

A reset cycle is carried out after the supply voltage has come up. After the reset cycle access to the I²C registers of the VM-012 is possible after a delay of approx. 100 ms.

A sensor reset can also be initiated by software. For that the bit *AUTO_SENSOR_RESET* is set to 1. The bit is cleared automatically at the end of the sensor's reset cycle.

The image sensor can be held in reset state permanetly. During this state, the sensor's power supply is switched off. This can be used to reduce the power consumption of the camea module.
The sensor is brought in this state by setting the bit *SENSOR_RESET* to 1. The sensor remains in this state until the bit is cleared by software.
When the bit is cleared, the sensor's power supply is switched on again by the internal power controller and reset is deasserted. After approx. 100 ms the sensor can be accessed again.

Notes:
- After a sensor reset is performed, the contents of the sensor registers are set to default state.
- Neither read or write access of sensor registers may be performed while the image sensor is in reset state.
- The VM012 control- and status registers which are mapped into the sensor's registers (see 5.7.5.3) can be accessed even while the sensor is performing a reset or is held in reset state.

A complete reset of the camera module can be performed by:
- powering the camera module off and on again
- by software: Asserting bit *VM-012_RESET*

A complete reset of the camera module can be initiated by asserting bit *VM-012_RESET*. The image sensor and the internal microcontroller will perform a reset cycle.
All registers are set to their default state.
The bit *VM-012_RESET* is automatically cleared at the end of the reset cycle.

Note:
Changes to the I²C address of the camera module take effect only after a complete reset of the camera module has been performed.

5.7.6.5 I²C-EEPROM (optional)

As an option, a serial I²C EEPROM can be installed on the VM-012 camera module. For example the EEPROM can be used to store application data such as calibration data.
The EEPROM type is M24C02-RMC6TG. It features a size of 2 kBit.
The default I^2C-address of the EEPROM is 0xAE.
Other addresses can be selected by setting J13, J14 and J15 (see section 5.6.2).
Data transfer rate: 100 kHz Standard Mode / 400 kHz Fast Mode

For more information please refer to the EEPROM's datasheet.

5.7.6.6 Internal MCLK Oscillator

As an option, the camera board can be populated with a crystal oscillator. This allows the generation of the master clock MCLK on board so no external MCLK clock has to be fed into the board on pin 29 of the phyCAM-P connector.
For using the internal clock source, OZ1 must be populated and J1 must be set to 1+2 position.

5.7.7 Development Kits

Development kits are available for various microprocessor platforms and operating systems for testing camera modules as well as application development. PHYTEC is continuously expanding the platforms supported in these kits. Please refer to the PHYTEC website for the latest information on available kits. Our sales and support team is ready to assist in selection of the appropriate kits and image processing hardware.

6 Design-In Guide

6.1 phyCAM-P

6.1.1 Design Considerations

The phyCAM-P interface is optimized for a flat interface design, enabling developers to select between a cost effective or compatibility and scalable design. The level of optimization can be chosen individually based on the following three primary considerations (see also *Table 35*):

- **Power Supply**
  The supply voltage of the various phyCAM-P cameras can vary. If a Carrier Board or target hardware application board is intended to support several different camera modules, the camera supply voltage must be adapted to the connected camera. This can be achieved by using a separate, variable voltage regulator that automatically adapts to the appropriate voltage for each camera by sensing the resistance on pin 31 of the camera connector (see circuit reference design below). In case only one dedicated camera is used, a separate regulator might not be needed.

- **Signal Level**
  According to the supply voltage, the level of signal lines (data-, control- and I²C-lines) can also differ between the different camera modules. For a universal circuit design, level shifter / translators must be inserted in theses lines. The level shifters translate the signal voltages on the microprocessor side to the voltage level of V_{CAM} on the camera side. In case the circuit design is made for one dedicated camera module, level shifters are only necessary if the signal level of the microprocessor circuitry differs from the signal level of the camera module.

- **Use of Camera Features**
  The different phyCAM-P camera modules offer various additional features, either on the camera module itself or as

additional signals over the *CAM_CTRL* pins on the phyCAM-P connector. These additional features may differ from camera to camera. Accordingly, the function of the *CAM_CTRL* pins differs. If the design is dedicated to one camera module, all additional features of the specific Carrier Board or application board can be used in the design. To best ensure compatibility, PHYTEC recommends using as few special features as possible. This minimizes the risk that a different camera module does not support a particular function and would therefore not be interchangeable on Carrier Board and target hardware application modules.

In some cases the polarity or signal type, such as edge of level triggered, might differ. We recommend adding (solder-) jumpers into the *CAM_CTRL* – lines. If CAM_CTRL pins are not used in a design, we recommend to use jumpers to establish the following connections:
CAM_CTRL_1: connect with jumper to GND/V_{CAM}
CAM_CTRL_2: connect with jumper to GND

Please ensure that application software is adapted to the different camera features.

The following table summarizes the main considerations for target hardware application board design:

phyCAM-P	Cost-optimized design	Compatible design
Power supply	Fixed power supply according to the camera model that is used	Variable power supply controlled by interface pin 31
Signal lines	Level shifter is only required if the signal level of target hardware application board differs from that of the camera module	Level shifter is always required
I²C-Interface	Level shifter is only required if the signal level of target hardware application board differs from that of the camera module	Level shifter is always required
Feature-pins (CAM_CTRL_1/2)	No limitations, features of the camera can be used according to application	Features may vary between different camera modules. Add jumpers for different options.

Table 35: phyCAM-P Design Considerations

6.1.2 Reference Design phyCAM-P

This section provides a reference design for phyCAM-P cameras, which offers high compatibility between the different modules.

The power supply is based on a variable voltage regulator (step-down type).

The low end of the feedback path is connected to the voltage selection resistor of the camera module (pin 31). This design can supply *VCC_CAM* with voltage values from 1.8V to 3.3V. It is designed for regulators with a feedback reference voltage of 1.25V. However the circuit can be adapted to regulators with different reference voltages by changing the resistor values of R100, R101 and R102, R103. As needed, C103 can be added to suppress noise or unwanted oscillation response. Please note that too high a capacitance value can negatively influence the loop response control behavior.

For circuit design and PCB layout, please consider the design guidelines of the regulator device deployed in the target hardware application board circuitry. Ripple and high frequency noise on the output voltage may cause visible interferences in the camera signal.

Please see *Figure92* for a design example:
U101 is a level shifter that adapts the signals coming from the

microprocessor, or circuitry on the target hardware application board, to the camera (outgoing signals).
In the reference design, these signals are the master clock *MCLK* and the reset signal.

Note that, in this particular example, the levels of the two input signals *x_CSI_MCLK* and *x_/RESET_3V3* already differ from one another. In this case *VCC_CSI* is lower than 3.3V, which is the high-level of the reset signal. In order to feed both signals through the same level shifter at U101 (the A-side of which is at *VCC_CSI* level), the slow reset signal is adapted by the voltage divider at R104 / R105 to the *VCC_CSI*-level.

The level shifter at U102 then converts the incoming signals from the camera to the level of the microprocessor's camera interface (*VCC_CSI*). The signals are fed to the camera interface by the *CAMERA* bus.

A bidirectional level shifter is needed for the I²C bus . The voltage level of the I²C bus on the target hardware application board might differ from the voltage level of the processor's camera interface. Therefore the voltage of the I²C bus is labeled as *VCC_I2C*. It is recommended to use only one set of pull-up resistors per I²C - bus segment. Multiple pull-up resistor on the same line may cause malfunction of the serial interface.

Note:
Bidirectional level shifters usually use differing threshold levels to avoid latch-up situations of the line.

If multiple level shifters are connected to a bus, or level shifters are connected in serial, this may lead to undesired side effects. In addition, some devices might not recognize the lower signal levels on the bus.

In the circuit reference design shown below, VCC_I2C must not be lower than 2.7V. We strongly recommend referring to the datasheets of the level shifters, as well as designing circuitry in accordance with recommendations within these datasheets.

CAM_CTRL signals are not used in this circuit reference example. The four-position jumpers J100 / J101 allow connecting the CAM_CTRL signals to either VCC_CAM, GND or a special function circuit on the target hardware application board. Please note that these signals might also need level translation.

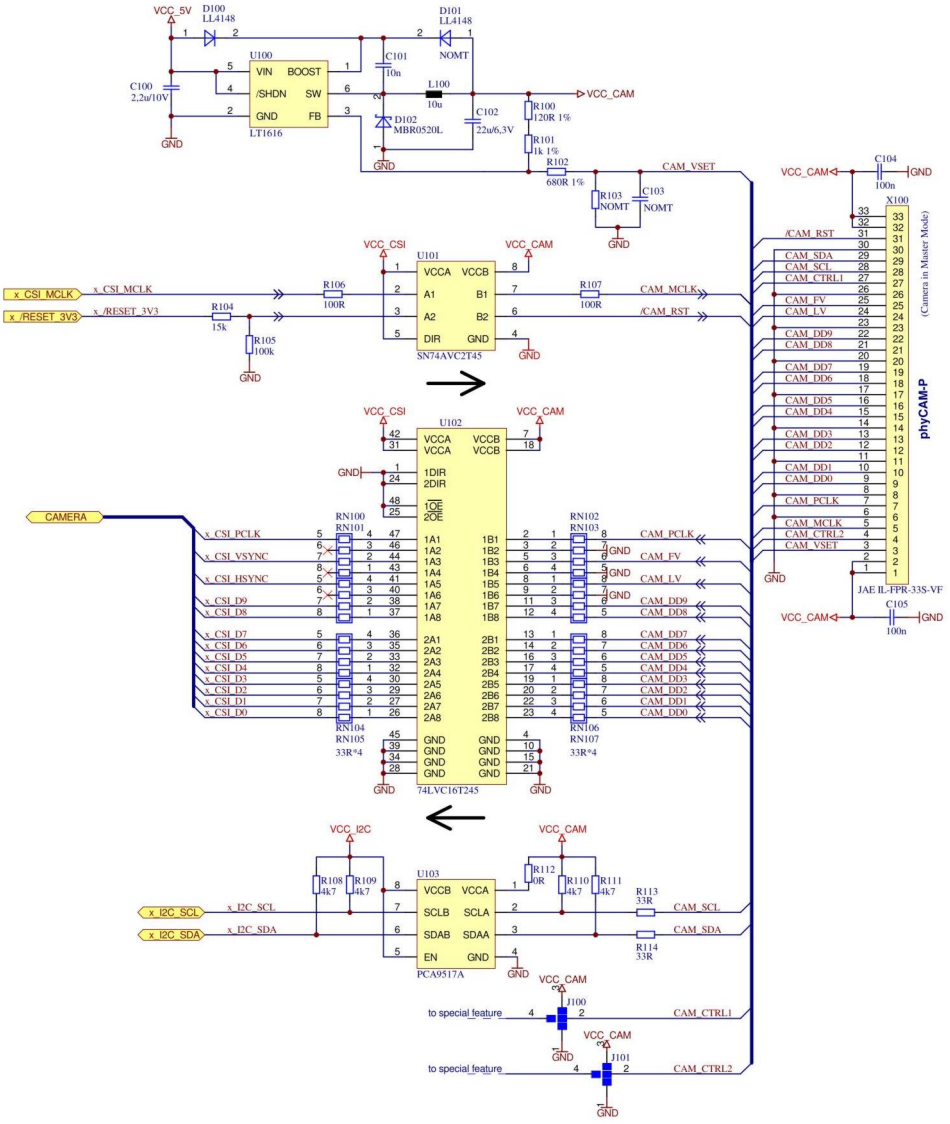


Figure92: Reference Circuitry: phyCAM-P Interface

Note:

- Please note that the pin numbering of the phyCAM-P connector on the standard PHYTEC Carrier Board is mirrored in relation to the camera. This is the case if FFC cables are used, which have contact stripes on the same side. Cables with contacts on opposite sides (upper and lower side) usually do not mirror the pin assignment. We recommend checking the pin numbering of the design with respect to the connectors and cable types that are used.
- Depending on the application as well as mounting and housing situation, additional measures might be necessary to meet EMI requirements as well as to provide protection against electrostatic discharge.

6.2 phyCAM-S/S+

This section provides different reference designs for phyCAM-S camera modules.

Since the phyCAM-S interface is designed for a high-level of compatibility, there is no need to provide for differing signal levels on the data lines. phyCAM-S cameras have a supply voltage of 3.3 V. This is the same signal level as for the serial I²C interface. Image data and master clock are transmitted as LVDS-signals. Accordingly, the LVDS driver and serializer/deserializer signal levels on the standard Carrier Board automatically adapt.

The following reference circuitry designs are presented in this section:

- A phyFLEX Carrier Board for connection with an internal phyCAM-S camera located within housing
- A phyFLEX Carrier Board for connection to an external phyCAM-S camera connected by a cable
- Carrier Board using any desired PHYTEC SOM - not only phyFLEX family SOM - featuring a parallel camera interface

The reference circuitry can also be used for designs deploying a **phyCARD** SOM with a serial camera interface.

6.2.1 Mixing phyCAM-S and phyCAM-S+

The phyCAM-S+ interface was desiged to be compatible with the phyCAM-S interface. Both phyCAM-S and phyCAM-S+ products can be used in the same design (which means they can be mixed in a design).

When mixing phyCAM-S and phyCAM-S+, only the different specifications of the pixel clock have to be taken into consideration:

- A phyCAM-S camera can connect to a SOM with a phyCAM-S+ interface if the minimum clock frequency of *PCLK* is higher than 20 MHz

- phyCAM-S+ cameras can connect to a SOM with a phyCAM-S interface if the maximum *PCLK* frequency is lower than 40 MHz.

Please see sections **Fehler! Verweisquelle konnte nicht gefunden werden.** and **Fehler! Verweisquelle konnte nicht gefunden werden.** for details.

6.2.2 Reference Design phyCARD / phyFLEX – Carrier Board, internal phyCAM-S/S+ camera

Almost all phyCARD- and phyFLEX- SOMs already feature a serial LVDS camera interface. The LVDS data lines from the camera are directly fed to the phyCARD/phyFLEX module. This makes it easy to design in a phyCAM-S/S+ camera in an application in which a phyCARD/phyFLEX is deployed.

The reference circuitry below requires only two active components:

Power: A simple 3.3 V power source is sufficient to supply the camera. The supply should provide a minimum of 500 mA. In the following reference circuitry, simple fliter networks are used to remove high frequency noise. Depending on the application,

additional measures for EMI suppression might be necessary. To source a master clock to the camera, an LVDS driver must be provided on the target hardware application board.

phyCARD/phyFLEX modules supply the clock as an asymmetrical signal with the voltage level *VCC_LOGIC* (phyCARD interface pin 16A, phyFLEX i.MX6 *VCC_LOGIC* =3.3V). The LVDS driver chip shown in the reference circuitry below functions with all phyCARD/phyFLEX SOMs that have a logic-high – level of + 2.0V or above.

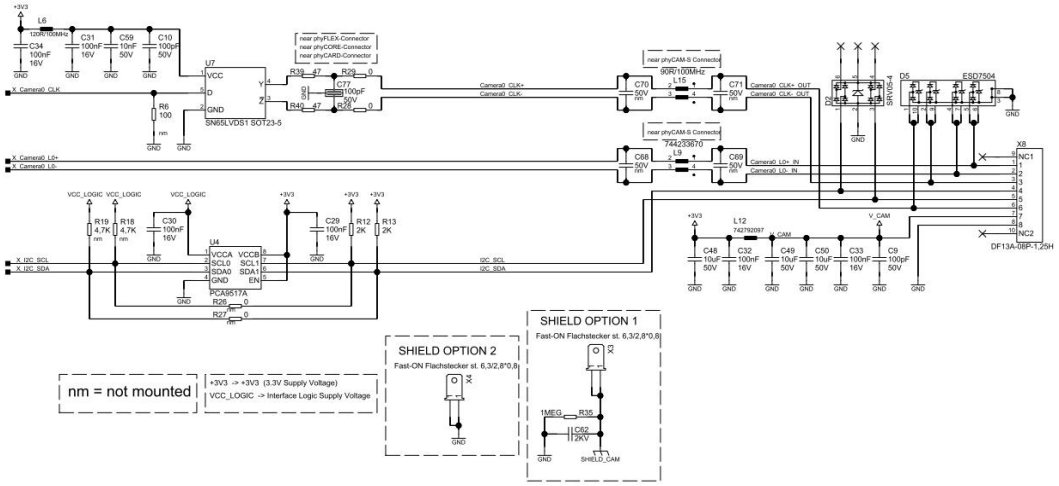


Figure93: Reference Circuitry: internal phyCAM-S at phyCARD Carrier Board

I²C Level-Shifter: The level shifter at U4 converts the levels of the I²C interface. The serial interface signal level on the camera is always at 3.3 V, but can be different on the phyCARD/phyFLEX SOM. *VCC_LOGIC* defines the I²C level of the SOM. The level shifter shown in the reference circuitry operates within a voltage range of 0.9V to 5.0V for *VCC_LOGIC*.

It is recommended to use only one set of pull-up resistors per I²C - bus segment. Multiple pull-up resistors on the same line may cause malfunction of the serial interface.

Note:
Bidirectional level shifters usually use differing threshold levels to avoid latch-up situations of the line.

If multiple level shifters are connected to a bus or level shifters are connected in serial, this may lead to undesired side effects. In addition, some devices might not recognize the lower signal levels on the bus.

We strongly recommend referring to the datasheets of the level shifters, as well as designing circuitry in accordance with recommendations within these datasheets.

In this reference circuitry the camera is located inside device housing. Therefore a short cable is only needed to connect the camera and the target hardware application board.

For connectivity, PHYTEC recommends a miniature Hirose DF13A-8P-1.25H connector. This is the same connector used on the camera module. Accordingly, both the camera and target hardware application board can be populated with the same connector.

Please note that the camera cable must fulfill the twisted pair lead requirement of the LVDS interface. We recommend to use a shielded cable.
We recommend the use of surge protection / clamping diodes in the camera's data lines as shown in Figure95.

Layout requirements for LVDS signals:
The circuit paths of the LVDS channels must be differential and routed with the same spacing over the entire circuit path.
The spacing of the differential pair should be as small as possible. The length of the two, differential LVDS channels should be identical.
The impedance of a LVDS path should be between 90Ω and 110Ω, typically 100Ω. Vias should be avoided.

The layout can be optimized by placing the circuit path on the inner layers as strip lines. This improves EMI behavior of the design as well as reduces the electromagnetic radiation of the LVDS signals.

For more informations about circuit and PCB-optimization see the application note LAN-068

6.2.3 Reference Design phyCARD / phyFLEX – Carrier Board, external phyCAM-S/S+ camera

This reference circuitry is very similar to that described in the previous section. These circuitries differ in that the camera in this example is not located in the Carrier Board housing, but connected externally by a cable. For example, this would enable the camera module to be located in a portable camera head.

For camera connection, we use an RJ-45 connector (modular plug, 8P8C type, shielded).
The matching cable quality depends on the cable length, clock / data frequency and application requirements.
For example, CAT-5e, CAT-6 or (especially for higher frequencies) USB-3.0 rated cables could be suitable.

The design shown in *Figure94* is a slightly modified variant of the schematic shown in *Figure93*. Modifications are as follows:

- The camera connector is replaced by an RJ-45 connector.
- At the data lines, suppressor diodes at D3 / D6 are used to protect the circuitry against overvoltage / ESD events.
- U9 is added to the power supply path in order to achieve supply voltage protection and short circuit strength.

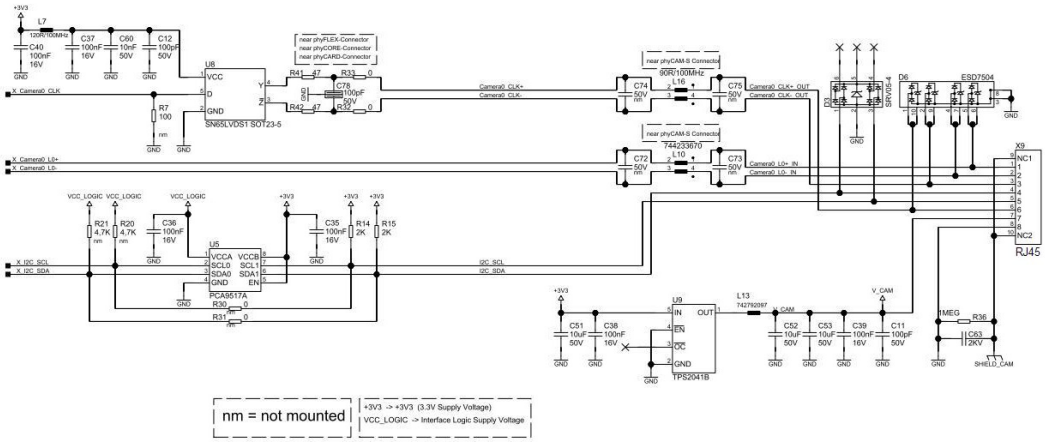


Figure94: Reference Circuitry: phyCARD/phyFLEX Carrier Board with external camera

Please note the design guidelines in 6.2.2.

The EMI / ESD protection measures shown in *Figure94* are for reference only. Depending on the application, as well as mounting and housing needs, additional measures might be necessary to meet EMI requirements.
Recommended clamping diodes for D3, D6:

- ON Semiconductor ESD7504
- Semtech SRV05-4

Please note that the RJ-45 connector used for the camera in this reference circuitry could be mistaken for another interface that uses the same connector type, such as Ethernet or a 1-Wire bus. Should distinction of interface types be a design requirement, we recommend using a different connector. The camera connection shown in the above reference circuitry is not designed for hot-plug ability. Additional circuitry is necessary to support hot-swap functionality.

6.2.4 Reference Design phyCAM-S/S+ at a parallel camera interface

A phyCAM-S/S+ can connect to any PHYTEC SOM that provides a parallel camera interface. However, this requires that image data sent by the camera in LVDS format be deserialized and converted to a parallel data stream.

As is the case with a phyCAM-P design, different voltage levels of the microprocessor must be taken into consideration.

Figure95 shows the camera externally connected with a CAT-5e cable.
Power supply and I²C interface are the same as in the reference schematic in the previous section. However, depending on the logic level of the microprocessor's I²C interface, a level shifter at U3 connects to supply voltage *VCC_I2C*.

U4 converts the master clock to an LDVS signal. The camera interface of the microprocessor (denoted as *X_CAMERA*) generates the master clock for the camera.

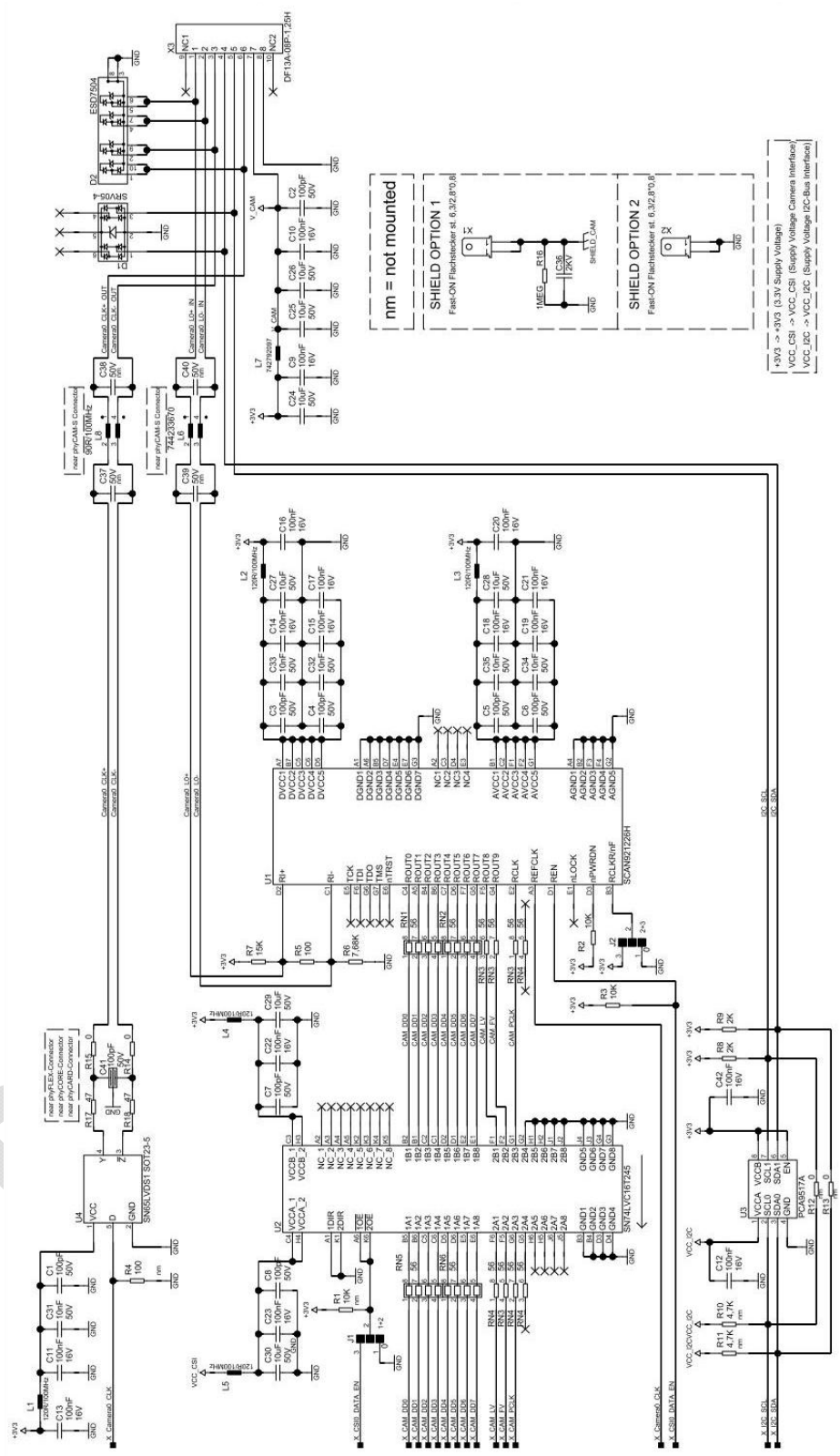


Figure95: Reference Circuitry: phyCAM-S/S+ at a parallel CPU camera interface

The reconversion of the camera image data is carried out in two steps:

- U1 deserializes the data from the camera to a parallel data stream. Bit 8 and Bit 9 represent the sync signals line valid and frame valid. Please ensure that the processor interface is configured to the appropriate signal polarity. This is also applicable for the pixel clock *CAM_PCLK*, which is recovered from the LVDS clock. Note that, in case the processor interface allows no adjustment, J2 can be used to select the clock polarity. Default state is RCLK= high → clock strobe rising edge. Since the clock is recovered from the LVDS signal, the clock polarity is not necessarily the same as on the camera side.

- In the second step, U2 adjusts the signal level to the processor interface *VCC_CSI*. This can be omitted if the processor camera interface is 3.3V compatible.

Please check in each individual use case whether the underlying level and timing parameters are compatible with the microprocessor. Please also pay attention to the timing configured on the camera side and the limits of the LVDS interface clock frequencies.

Recommended deserializers for U1:

- For phyCAM-S compatible designs:
  National Semiconductor DS92LV1212A
- For phyCAM-S+ compatible designs:
  Texas Instruments SCAN921226H

Recommended clamping diodes for D101, D102:

- ON Semiconductor ESD7504
- Semtech SRV05-4

Note:
Recommended parts are not having the same pinout. Please refer to the corresponding datasheets.

Design examples are shown for reference only. Please verify if designs are compatible with your system requirements.

Note:
PHYTEC products are subject to continuous improvement.
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Germany: www.phytec.de

PHYTEC would be pleased to consult with selection of the appropriate image processing hardware for your design.