

PRODUCT GROUP

REV

ISSUE DATE

P/N.:TCON(DV430FHM-NN1)

-LVDS Connector : PM.LVS.S040505101(UJC) or Equivalent.

< Table 5. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No connection	21	GND	Ground
2	SDA	I ² C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I ² C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	No connection
5	NC	Not Connected	25	NC	No connection
6	NC	Not Connected	26	NC	No connection
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	No connection
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			

SPEC. TITLE

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Pin No	Symbol	Description	Pin No	Symbol	Description
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC	Not Connected	48	VCC	Input Voltage +12V
43	NC	Not Connected	49	VCC	Input Voltage +12V
44	GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

Notes : Notes : 1. NC(Not Connected) : This pins are only used for BOE intern al operations.

2.Input Level of LVDS signal is based on the EIA-644 Standard.

3. LVDS_SEL: This pin is used for selecting LVDS signal data format.

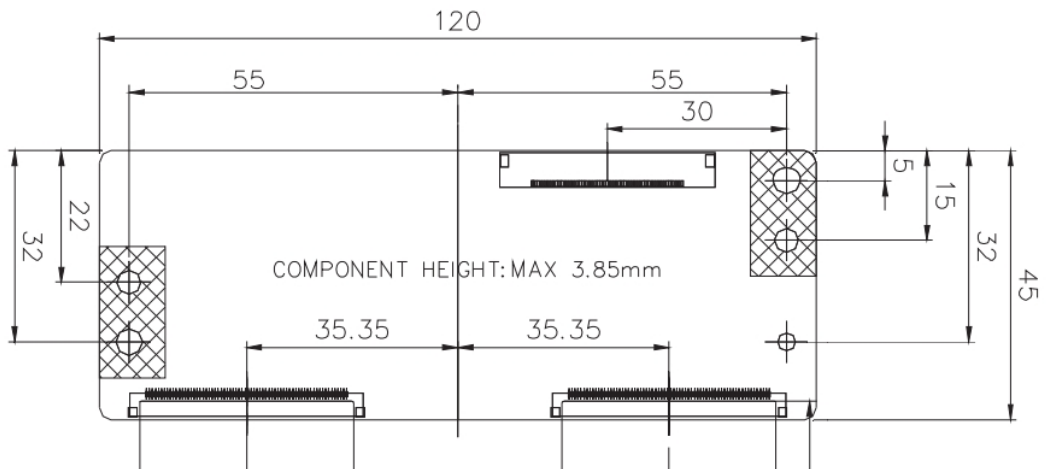
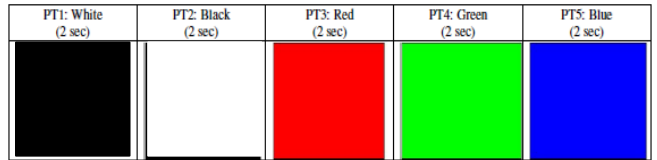
If this Pin : High (3.3V) JEIDA LVDS format

Otherwise : Low(GND) or Open (NC) Normal NS LVDS format

Rear view of LCM



BIST Pattern



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