650V GaN FET

Datasheet
Preliminary

1. Description

The G2N65 series FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.

Features

- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±20V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_g and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all SiC and GaN FETs for low loss during dead-times.
- Negligible Q_{rr} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.

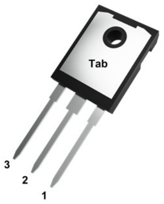
Benefits

- Enable very high conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced cooling requirements.
- Improved safety & reliability due to cooler operation temperature.
- Higher output power due to the best efficiency and thermal capability.

Applications

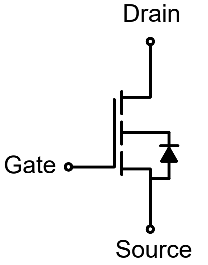
- Half-bridge buck/boost, totem-pole PFC circuits or inverter circuits.
- High-efficiency/High-frequency phase-shift, LLC or other soft-switching topologies.

Top View



Bottom View

Gate	1
Source	2, Tab
Drain	3



Schematic Symbol

Key Performance Parameters	
V_{DSS} (V)	650
$V_{DSS(PK),\ nonrepetitive}$ (V) [a)]	800
$V_{DSS(PK),\ repetitive}$ (V) [b)]	750
$R_{DS(on),\ typ}$ (mΩ) [c)]	35
Q_{oss} (nC)	150
Q_g (nC)	38

[a)] Duty cycle < 1%, spike duration < 30μs, nonrepetitive
[b)] Duty cycle < 1%, spike duration < 30μs, repetitive
[c)] Dynamic on-resistance

*Lead plating Pb-free
in compliance with RoHS

Part Number & Package Information

Part #	Package	Package Base
G2N65R035TB-H	TO-247-3L	Source

2. Maximum Ratings

Symbol	Parameter	Value
V_{DSS} (V)	Drain-source maximum voltage (T_J = -55°C to 150°C)	650
$V_{DSS(PK),\ nonrepetitive}$ (V)	Drain-source maximum peak voltage, nonrepetitive [a]	800
$V_{DSS(PK),\ repetitive}$ (V)	Drain-source maximum peak voltage, repetitive [a]	750
$V_{GSS,\ DC}$ (V)	Gate-source maximum voltage	±20
$V_{GSS,\ AC}$ (V)	Gate-source maximum voltage ($f \geq$ 50Hz)	±30
P_D (W)	Maximum power dissipation (T_C = 25°C)	174
I_{DS} (A)	Maximum continuous drain current (T_C = 25°C)	49.8
	Maximum continuous drain current (T_C = 100°C)	31.5
$I_{DS\ (pulse)}$ (A)	Maximum pulsed drain current (T_C = 25°C) [b]	240
T_J (°C)	Operating junction temperature	-55 to 150
T_S (°C)	Storage temperature	-55 to 150
T_{sold} (°C)	Wave-soldering peak temperature [c]	260
M_d (N·cm)	Mounting Torque, M3 and M3.5 screws	70

[a] Duty cycle < 1%, spike duration < 30μs

[b] Pulse width = 10μs

[c] For 10 seconds, 1.6mm from the case

3. Thermal Characteristics

Symbol	Parameter	Typ.
$R_{\Theta JC}$ (°C/W)	Junction-to-case thermal resistance	0.72
$R_{\Theta JA}$ (°C/W)	Junction-to-ambient thermal resistance	40

4. Device Characteristics

T_J = 25°C unless specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$V_{GS(th)}$	Gate threshold voltage	3.0	3.5	4.0	V	$V_{DS} = V_{GS}$, I_D = 4.3mA
$R_{DS(on)}$	Drain-source on resistance [a]	-	35	41	mΩ	V_{GS} = 10V, I_D = 30A
		-	70	-	mΩ	V_{GS} = 10V, I_D = 30A, T_J = 150°C
I_{DSS}	Drain-source leakage current	-	3	30	μA	V_{DS} = 650V, V_{GS} = 0V
		-	20	-	μA	V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-source leakage current	-	-	100	nA	V_{GS} = 20V
		-	-	-100	nA	V_{GS} = -20V
C_{iss}	Input capacitance	-	2410	-	pF	V_{GS} = 0V, V_{DS} = 400V, f = 500kHz
C_{oss}	Output capacitance	-	150	-	pF	V_{GS} = 0V, V_{DS} = 400V, f = 500kHz
C_{rss}	Reverse transfer capacitance	-	10	-	pF	V_{GS} = 0V, V_{DS} = 400V, f = 500kHz
$C_{o(er)}$	Equivalent output capacitance (energy related)	-	220	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
$C_{o(tr)}$	Equivalent output capacitance (time related)	-	375	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
Q_g	Gate charge total	-	38	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 30A
Q_{gs}	Gate to source charge	-	13.3	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 30A
Q_{gd}	Gate to drain charge	-	13	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 30A
Q_{oss}	Output charge	-	150	-	nC	V_{GS} = 0V, V_{DS} = 0V to 400V
$t_{d(on)}$	Turn-on delay time	-	70	-	ns	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 30A, R_G = 18Ω, Z_{FB} = 120Ω at 100MHz, see Figure 13
t_r	Rise time	-	10	-	ns	
$t_{d(off)}$	Turn-off delay time	-	100	-	ns	
t_f	Fall time	-	12	-	ns	

[a] Dynamic on-resistance

Reverse Device Characteristics, T_J = 25°C unless specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Reverse current	-	-	31.5	A	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle
$I_{S\ (pulse)}$	Pulsed reverse current	-	-	90	A	V_{GS} = 0V, V_{SD} = 6V, pulse width ≤ 10μs, T_J = 150°C
V_{SD}	Reverse voltage [a]	-	1.9	-	V	V_{GS} = 0V, I_S = 30A
		-	1.4	-	V	V_{GS} = 0V, I_S = 15A
t_{rr}	Reverse recovery time	-	41	-	ns	I_S = 30A, V_{DD} = 400V, di/dt = 1000A/μs
Q_{rr}	Reverse recovery charge [b]	-	0	-	nC	

[a] Including the effect of dynamic on-resistance

[b] Excluding Q_{oss}

5. Typical Characteristics (T_C = 25°C unless specified)

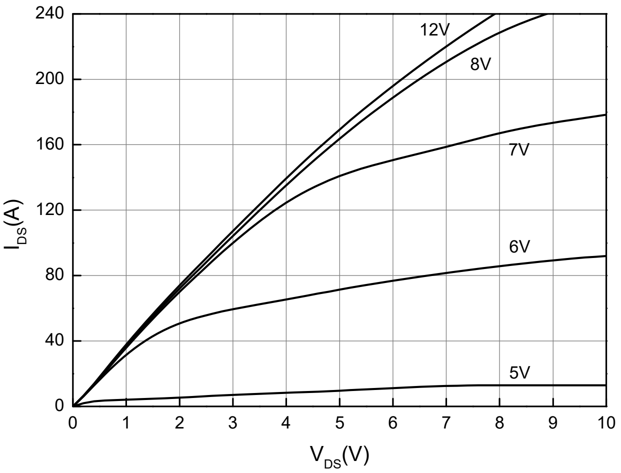


Figure 1. Typical Output Characteristics at T_J = 25°C (Parameter: V_{GS})

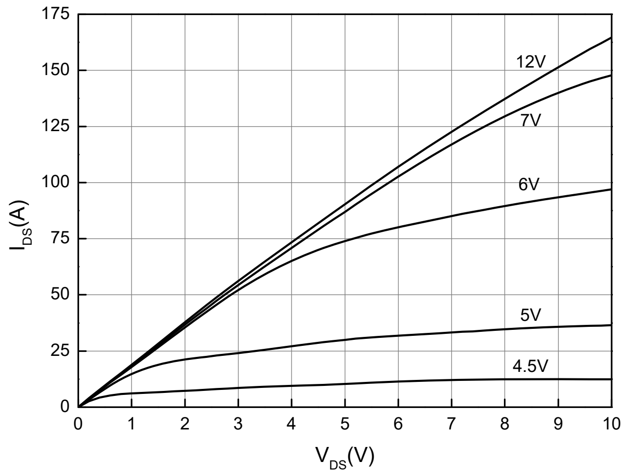


Figure 2. Typical Output Characteristics at T_J = 150°C (Parameter: V_{GS})

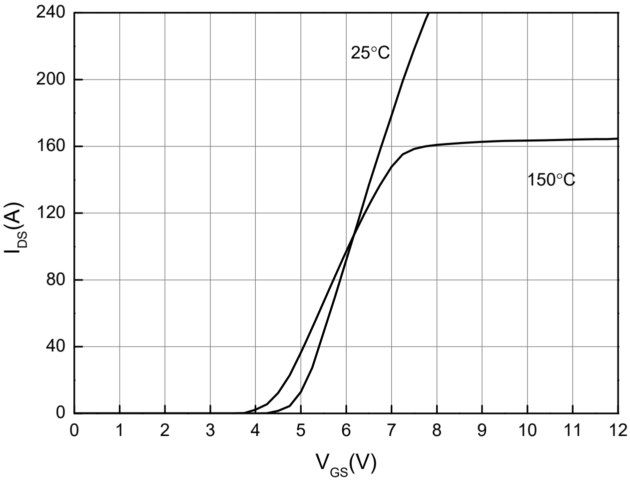


Figure 3. Typical Transfer Characteristics (V_{DS} = 10V, Parameter: T_J)

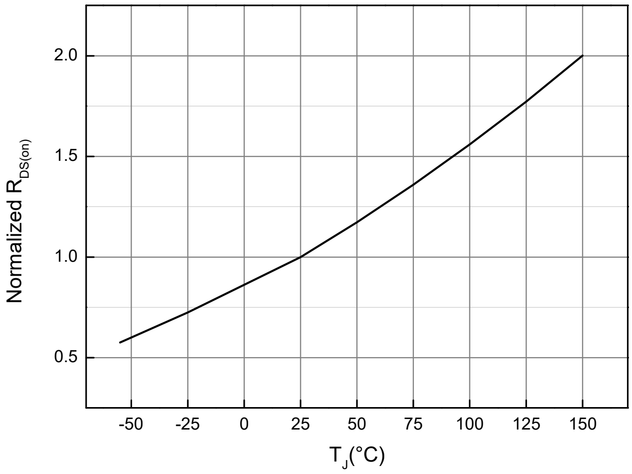


Figure 4. Normalized On-Resistance (I_D = 30A, V_{GS} = 10V)

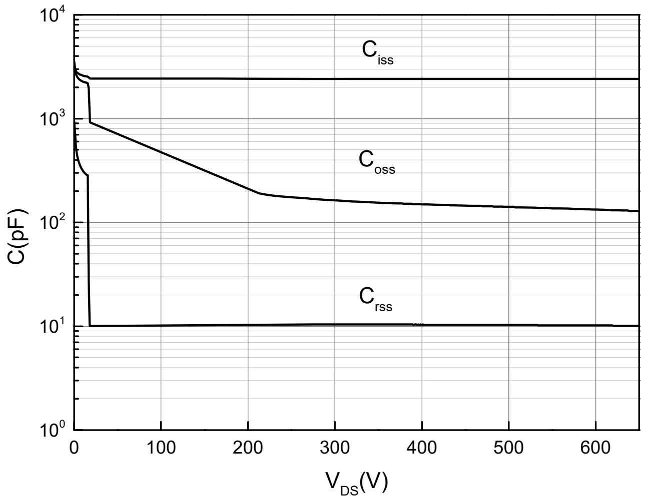


Figure 5. Typical Capacitance
(V_{GS} = 0V, *f* = 500kHz)

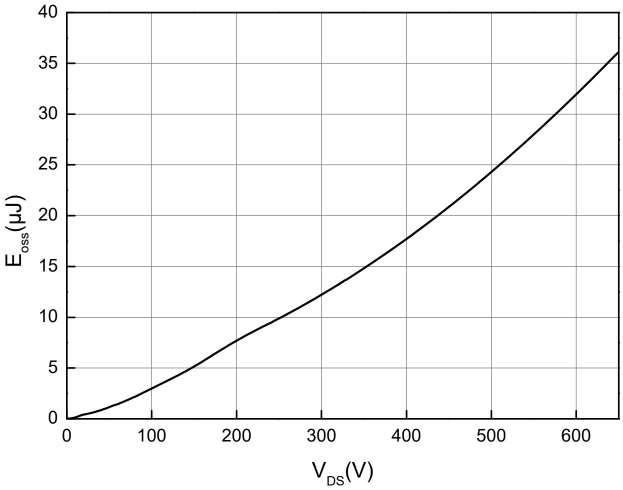


Figure 6. Typical C_{OSS} Stored Energy

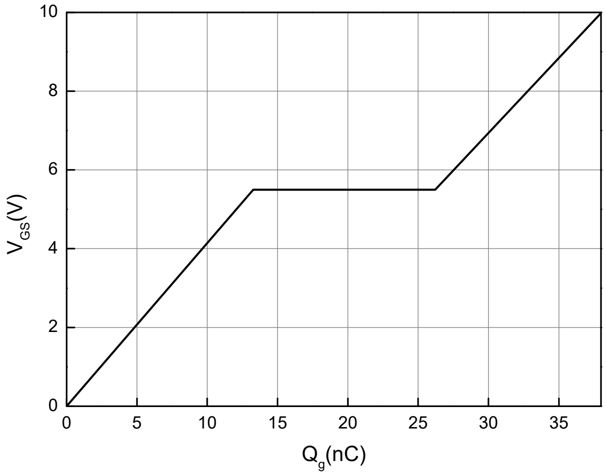


Figure 7. Typical Gate Charge
(I_{DS} = 30A, V_{DS} = 400V)

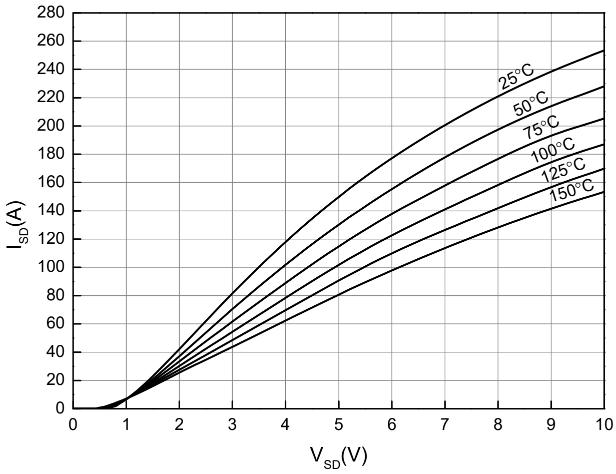


Figure 8. Reverse Conduction Characteristics
(-20V ≤ V_{GS} ≤ 0V, Parameter: T_J)

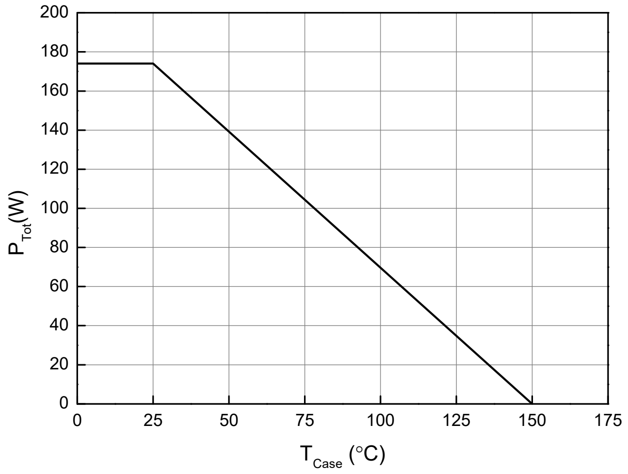


Figure 9. Power Dissipation

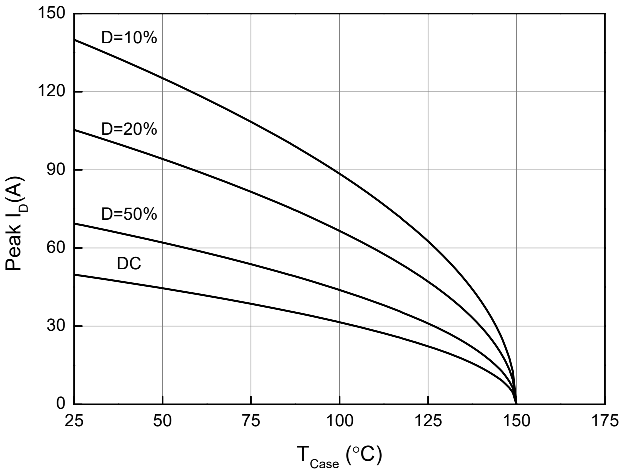


Figure 10. Current Derating

(Pulse Width ≤ 10μs, V_{GS} ≥ 10V)

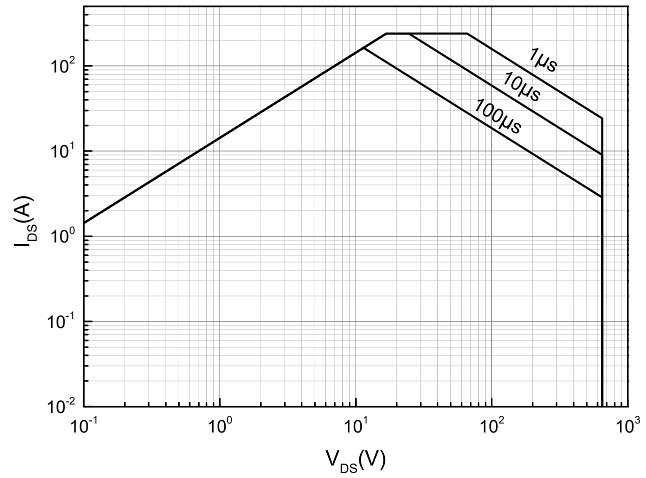


Figure 11. Safe Operating Area at T_C = 25°C

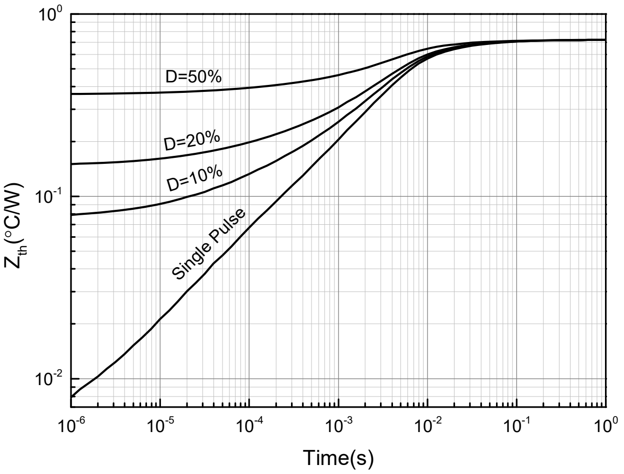


Figure 12. Transient Thermal Resistance

6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

DO	DO NOT
Place gate driver close to the GaN device and separate input traces from output traces	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor

7. Circuit Implementation

Half-bridge Schematic

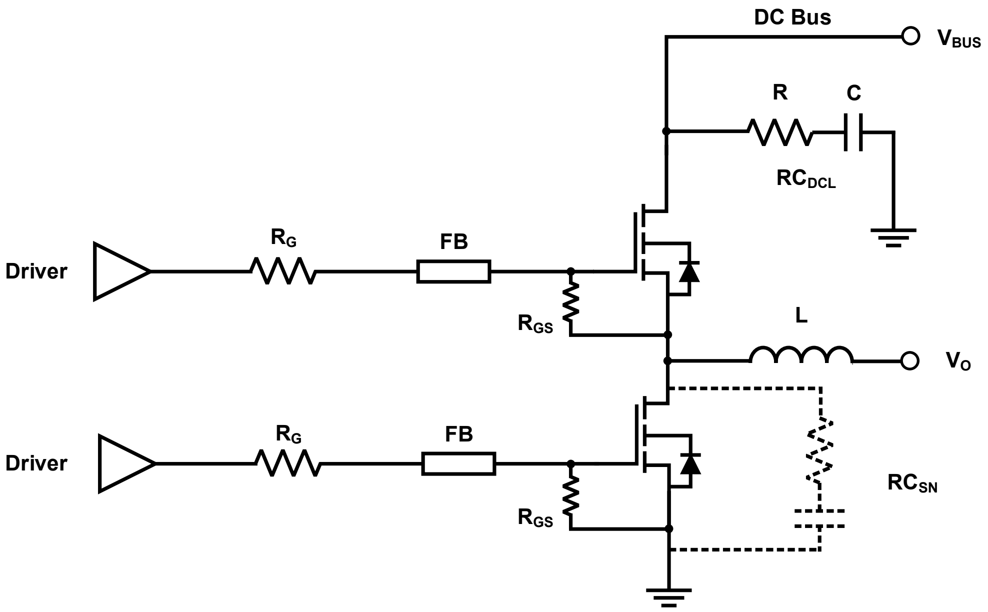


Figure 13. Simplified half-bridge schematic

Recommended gate drive: (0V, 12V) with $R_G = 18\Omega$ [a]

Gate Ferrite Bead (FB) [b]	Required DC Link RC Snubber (RC_{DCL}) [c]	Recommended Switching Node RC Snubber (RC_{SN})
120-180Ω @ 100MHz	(10-20nF + 3-5Ω) × 2	Not necessary, see note **d** and **e** below

Notes:

[a] For bridge topologies only. R_G could be smaller in single ended topologies.

[b] Examples of material selection: MPZ2012S***AT000(TDK), BLM21PG***SZ1D(Murata).

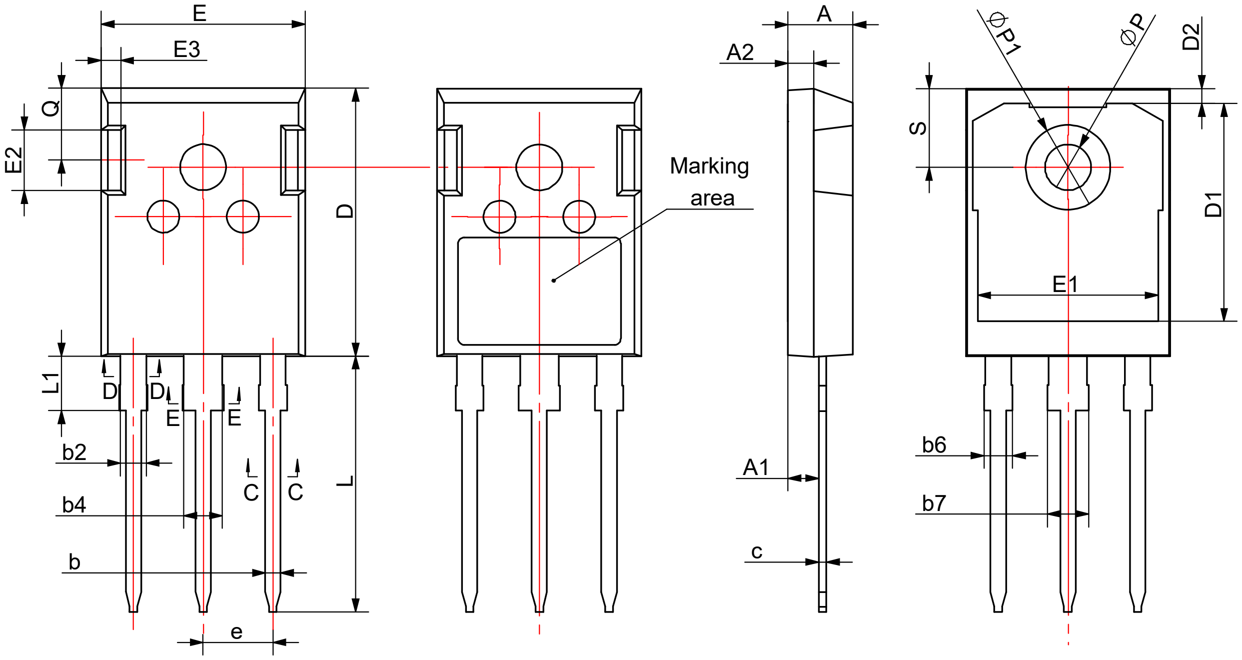
[c] RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitor(s) should be located away from the RC_{DCL}.

[d] RC_{SN} is needed only if R_G is smaller than recommendations.

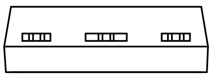
[e] If required, please use 10Ω+100pF.

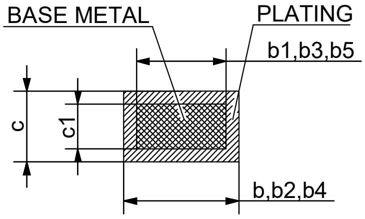
[f] The typical value of R_{GS} is 10kΩ.

8. Package Dimensions



SUPPLIER "A" PACKAGE SUPPLIER "B" PACKAGE





SECTION C-C,D-D & E-E

NOTES:

1. DIMENSIONS D & E NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.

2. LEAD FINISH UNCONTROLLED IN L1.

3. OUTLINE CONFORMS TO JEDEC TO-247-AD.

DIM.	Millimeters	
	MIN.	MAX.
A	4.82	5.21
A1	2.20	2.57
A2	1.82	2.18
b	1.07	1.35
b1	1.07	1.30
b2	1.87	2.41
b3	1.87	2.27
b4	2.87	3.38
b5	2.87	3.18
b6	—	2.25
b7	—	3.25
c	0.50	0.68
c1	0.50	0.65
D	20.67	21.11
D1	16.25	17.65
D2	0.81	1.35
E	15.70	16.15
E1	13.10	14.25
E2	3.68	5.10
E3	1.00	2.43
e	5.45BSC	
L	19.55	20.38
L1	3.93	4.48
P	3.40	3.69
P1	7.00	7.40
Q	5.41	6.00
S	6.04	6.30
TO-247-3L		
GaNext		
DATE: 2022.11		Rev. 03

9. Part Marking